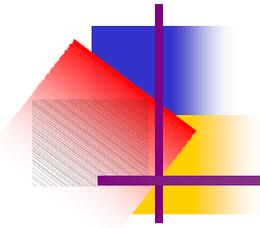


A Performance Modeling and Simulation Approach to Software Defined Radio

OMG Real-time & Embedded Systems Workshop
Washington, DC, July, 2005

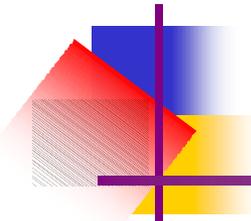
Long Ho & Shawkang Wu
Integrated Defense Systems
The Boeing Company
Anaheim, CA





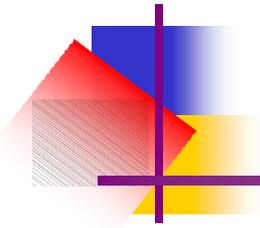
Typical M&S Approach

- Descriptive Analysis
 - Problem formulation
 - Input source collection and analysis
 - Model development, verification and validation
 - Scenario simulation and performance evaluation



Problem Formation

- Capability Verification
 - Verify that the capacity of the hardware architecture satisfies the operational need of the radio and waveform software for a particular JTR Set configuration
- Performance Analysis
 - Analyze end-to-end latency, component throughput, data and control bottlenecks meets resource loading and critical timing requirements
- Portability Validation
 - Validate that a particular waveform is properly partitioned
 - to match the capacity of the available hardware resources
 - to maximize software portability while satisfying application performance



Input Source Collection and Analysis

- Source Collection

- Documents

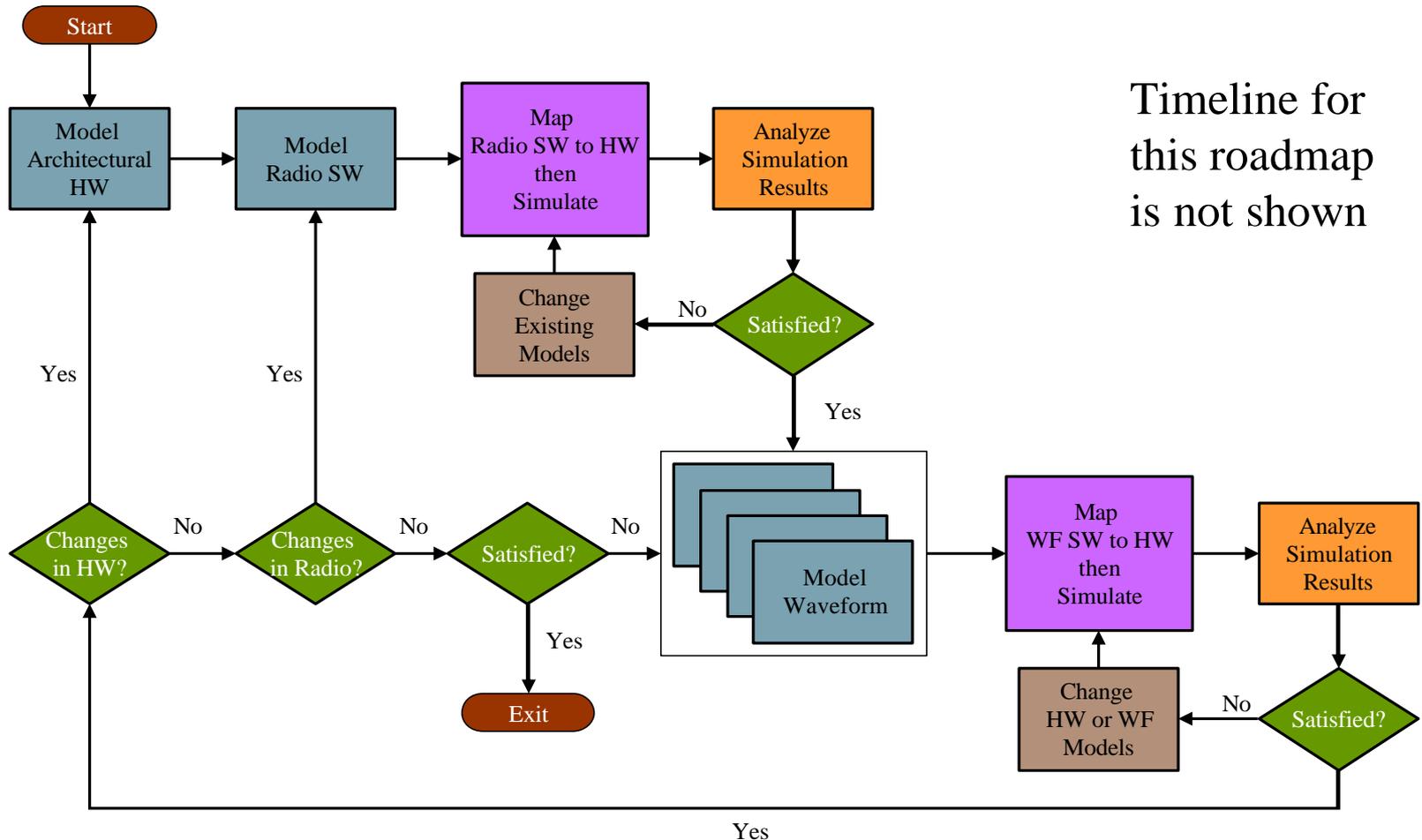
- SCA and its Supplements
 - RTOS, CORBA specifications
 - Waveform application specification
 - Radio application specification
 - JTR architecture specification

- Estimate and measure performance parameters

- Source Analysis

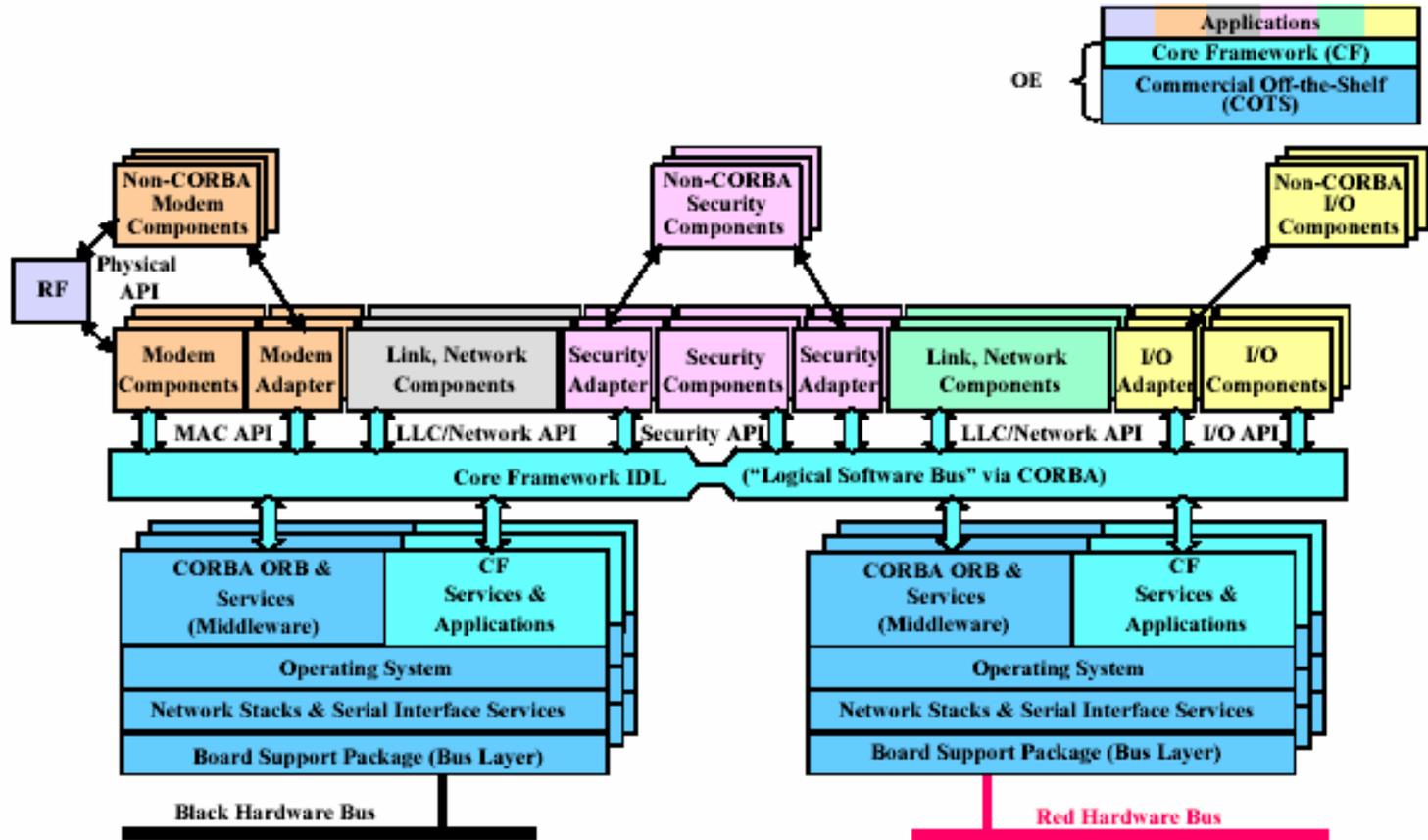
- Identify controllable and uncontrollable inputs
 - Identify constraints on the decision variables
 - Define system performance measure

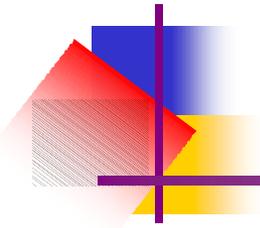
Model Development Roadmap



Timeline for this roadmap is not shown

SCA Architecture

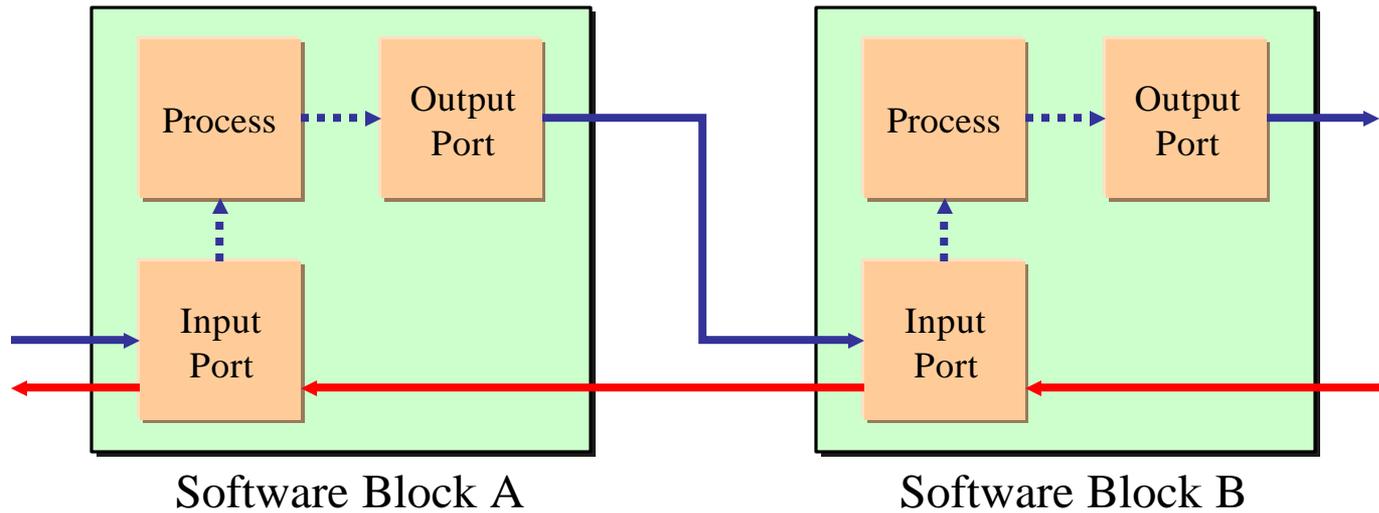




Modeling of Hardware Architecture

- The architectural model describes the hardware resources used in processing or transporting the radio and waveform application data
 - Create Models of Resource Building Blocks
 - Build Models of HW Components
 - Generate Models of HW Architecture
- Inputs for HW architecture model are from JTR hardware specifications
- Simulation parameters for a HW component are resource name and capacity

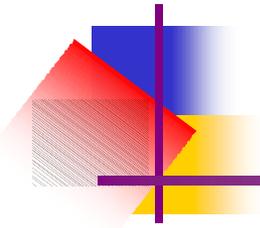
SCA Generic Building Block



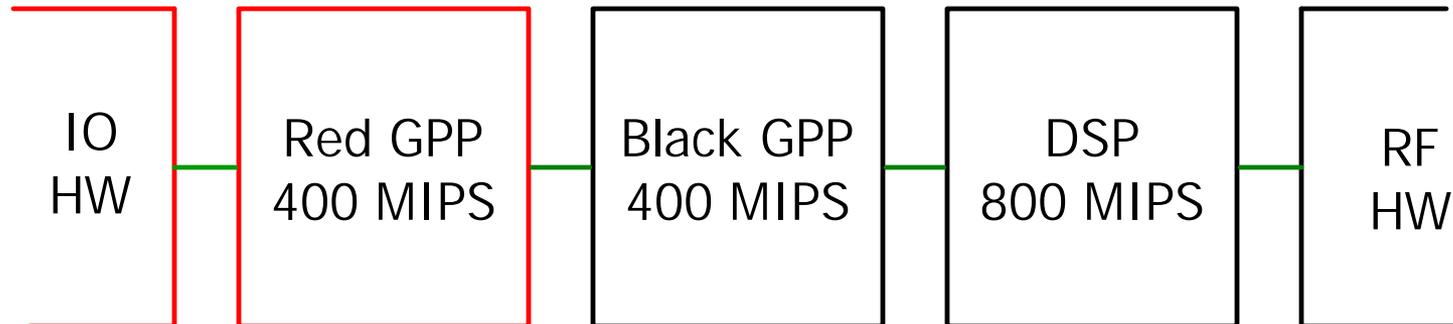
.....> Internal Data Flow (Small Latency)

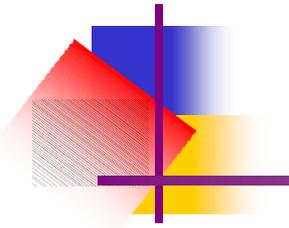
————> External Data Flow (Large Latency)

————< Control Flow



JTR Set Architecture





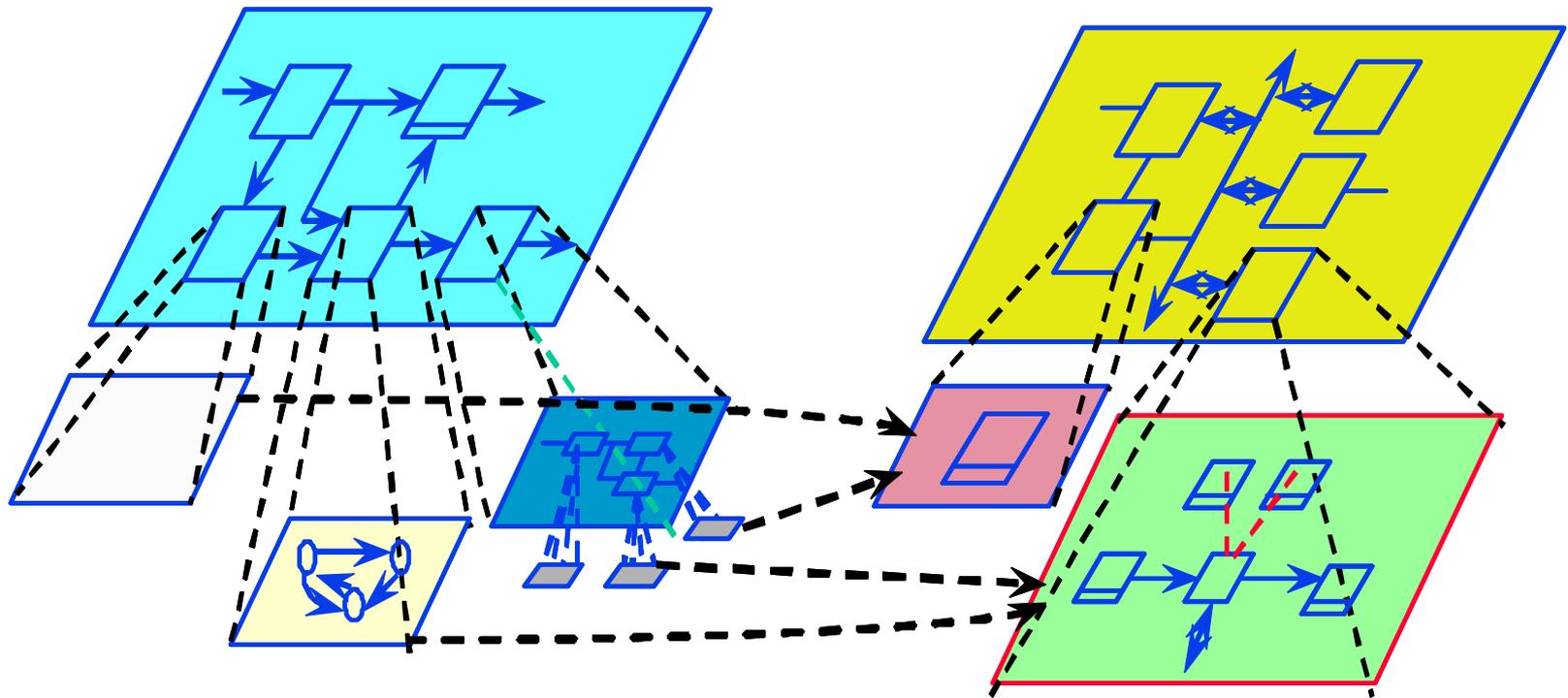
Tool Selection

- Co-Design tools provide two orthogonal views of a system
 - Architecture and function Views - which are linked by a partitioning specification
 - The capability for simulation of virtual system prototype
- A Co-Design tool by Foresight Systems

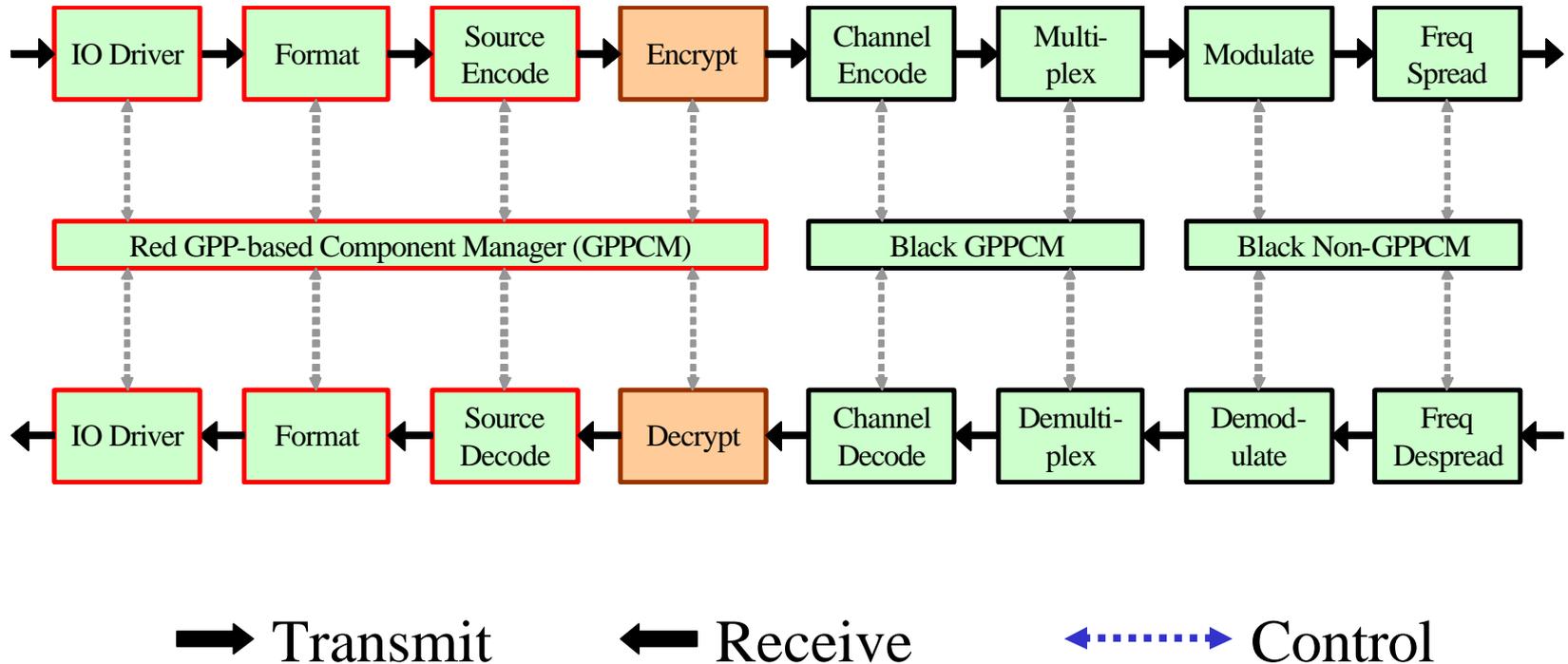
Functions to Architecture Mapping

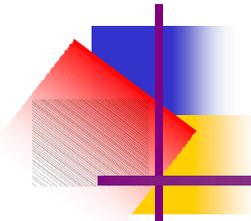
Functional Design

Architectural Design



Generic Communication Model





Scenario I - Simulation Configuration

- Utilization

- Red GPP

$$0.00375 \text{ sec} * 400 \text{ MI/sec} / 4 \text{ process} = 0.375 \text{ MI} / \text{process}$$

- Black GPP

$$0.00375 \text{ sec} * 400 \text{ MI/sec} / 2 \text{ process} = 0.75 \text{ MI} / \text{process}$$

- DSP

$$0.00375 \text{ sec} * 800 \text{ MI/sec} / 2 \text{ process} = 1.5 \text{ MI} / \text{process}$$

- Local Port

$$0.00125 \text{ sec} * 1/10 * 100 \text{ Mb/sec} = 0.0125 \text{ Mb}$$

- Remote Port

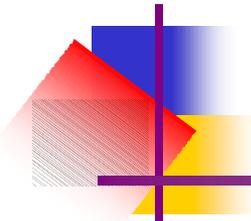
$$0.00125 \text{ sec} * 5/10 * 20 \text{ Mb/sec} = 0.00125 \text{ Mb}$$

- Total Latency

- Processor Delay + Local Transport Delay + Remote Transport Delay

$$= (3 * 0.00375) + (5 * 0.0125 \text{ Mb} / 100 \text{ Mbps}) + (3 * 0.0025 / 20 \text{ Mbps})$$

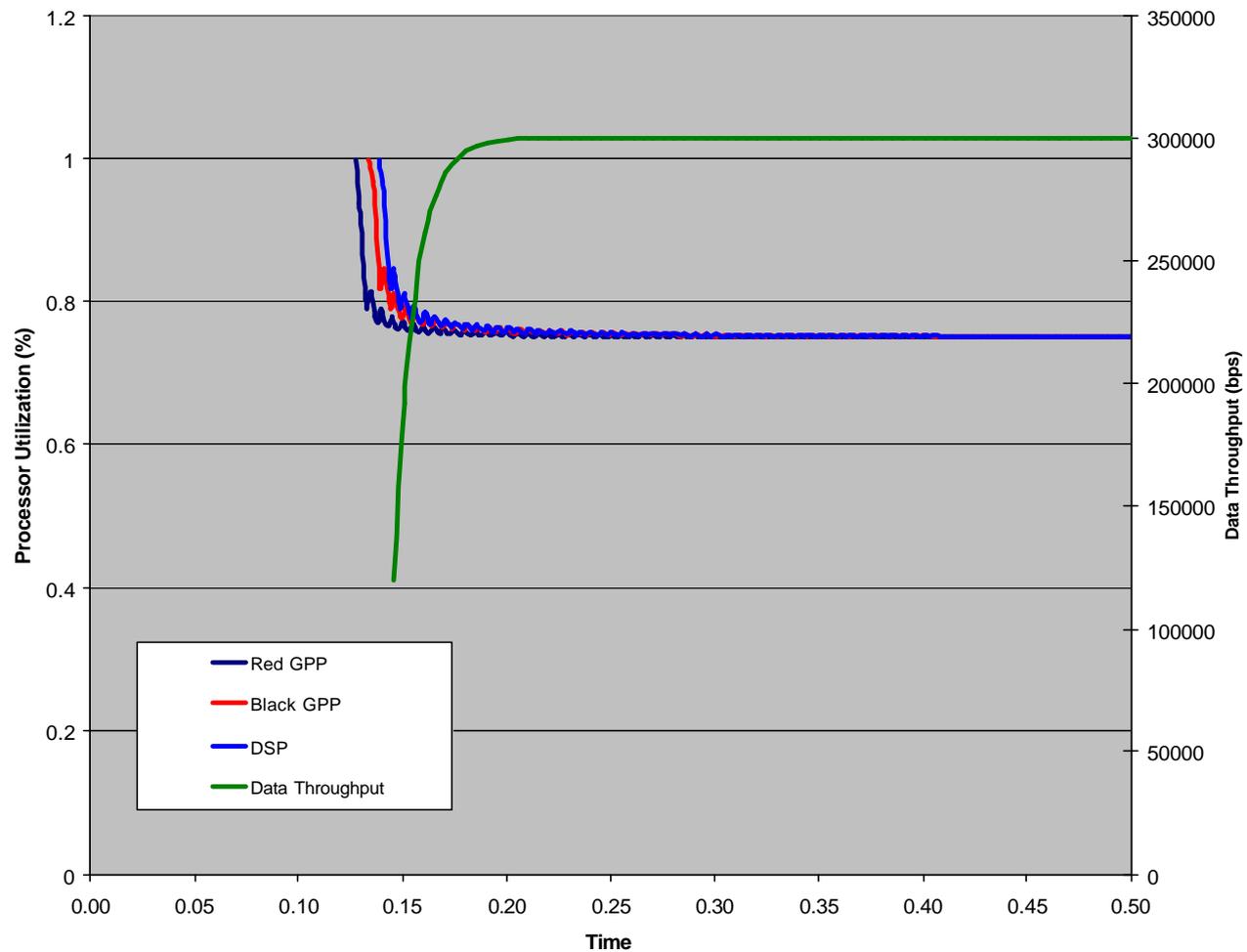
$$= 0.01125 + 0.000625 + 0.001875 = 0.01375 \text{ sec}$$



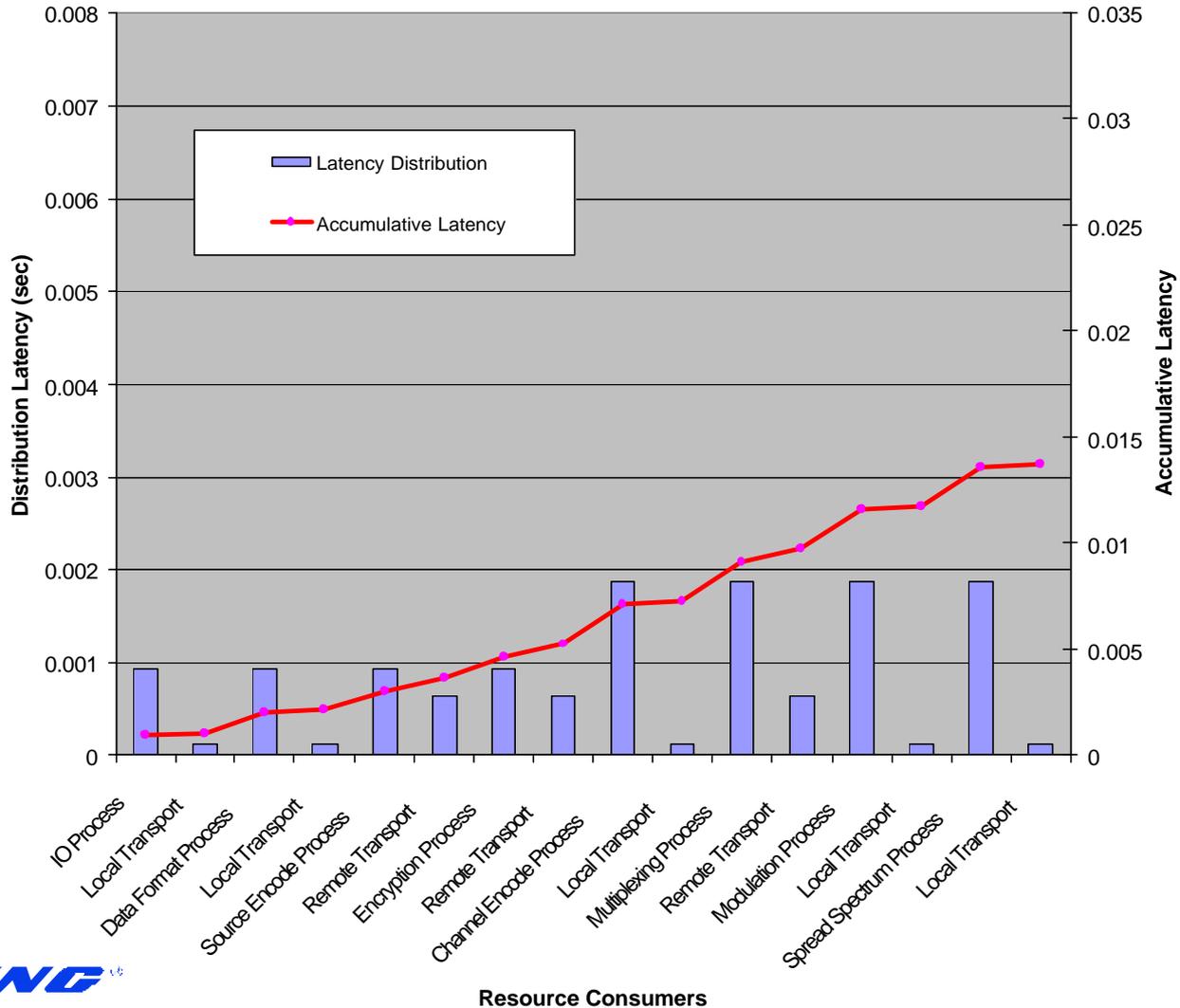
Case Studies

- Scenario II – Verify HW Capability
 - Reduce Black GPP from 400 to 200 MIPS
 - Data throughput reduced by 33%
 - Black GPP utilization increased to 100%
 - Latency increased by 68%
- Scenario III – Validate SW Portability
 - Re-map the modem software component from DSP resource to Black GPP resource
 - Data throughput reduced by 33%
 - Black GPP utilization increased to 100%
 - Latency increased by 119%

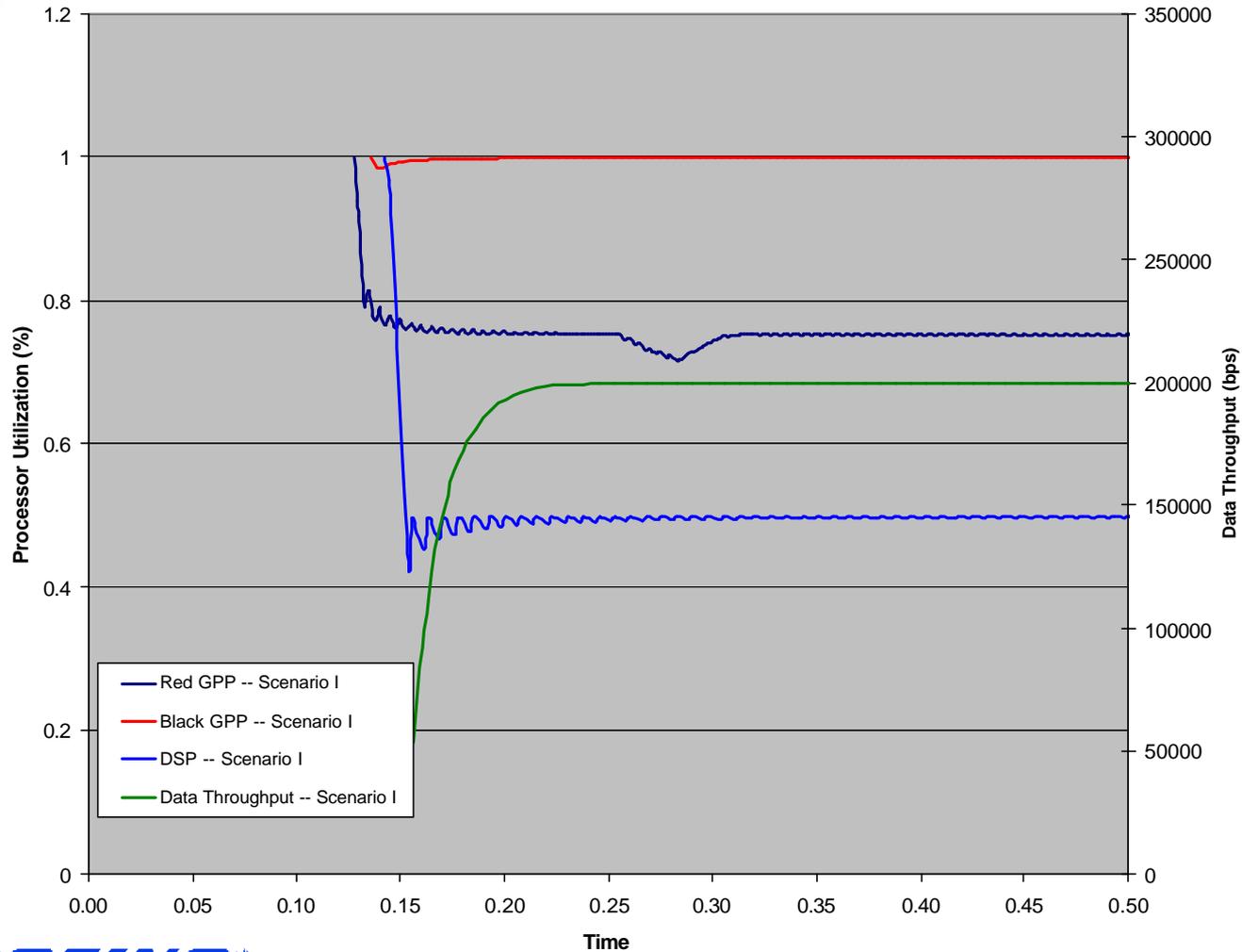
Scenario I – Resource Utilization



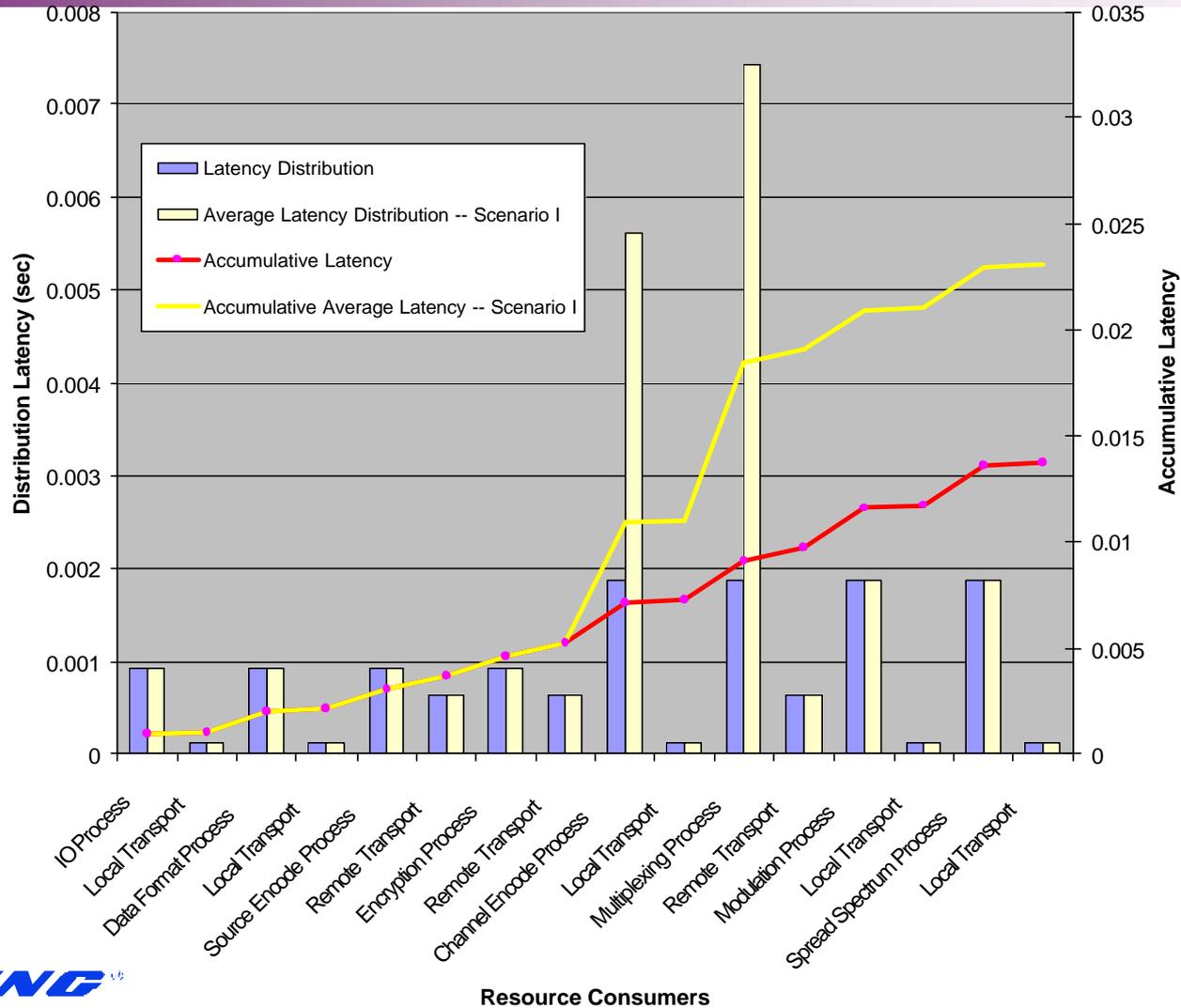
Scenario I – Latency



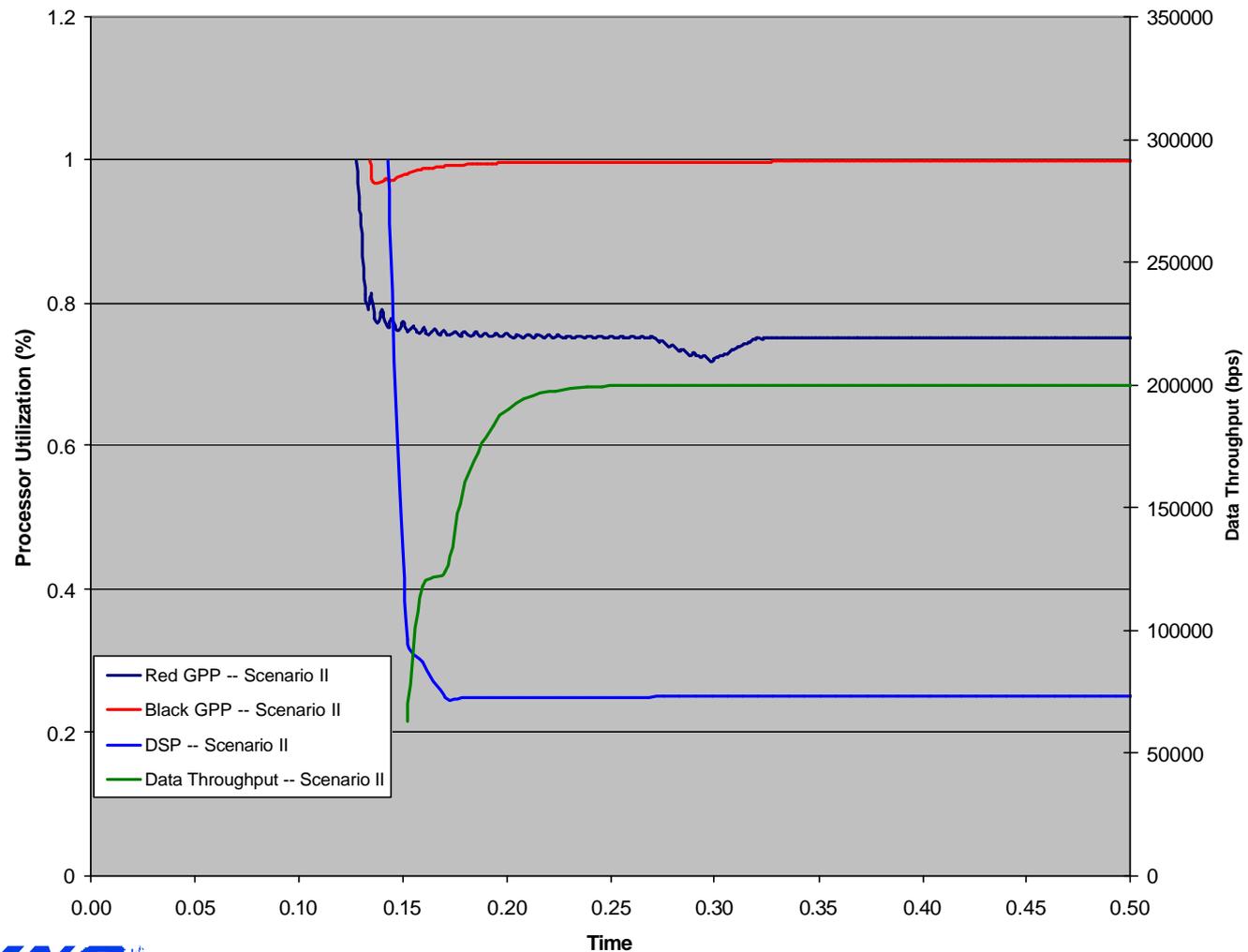
Scenario II – Resource Utilization



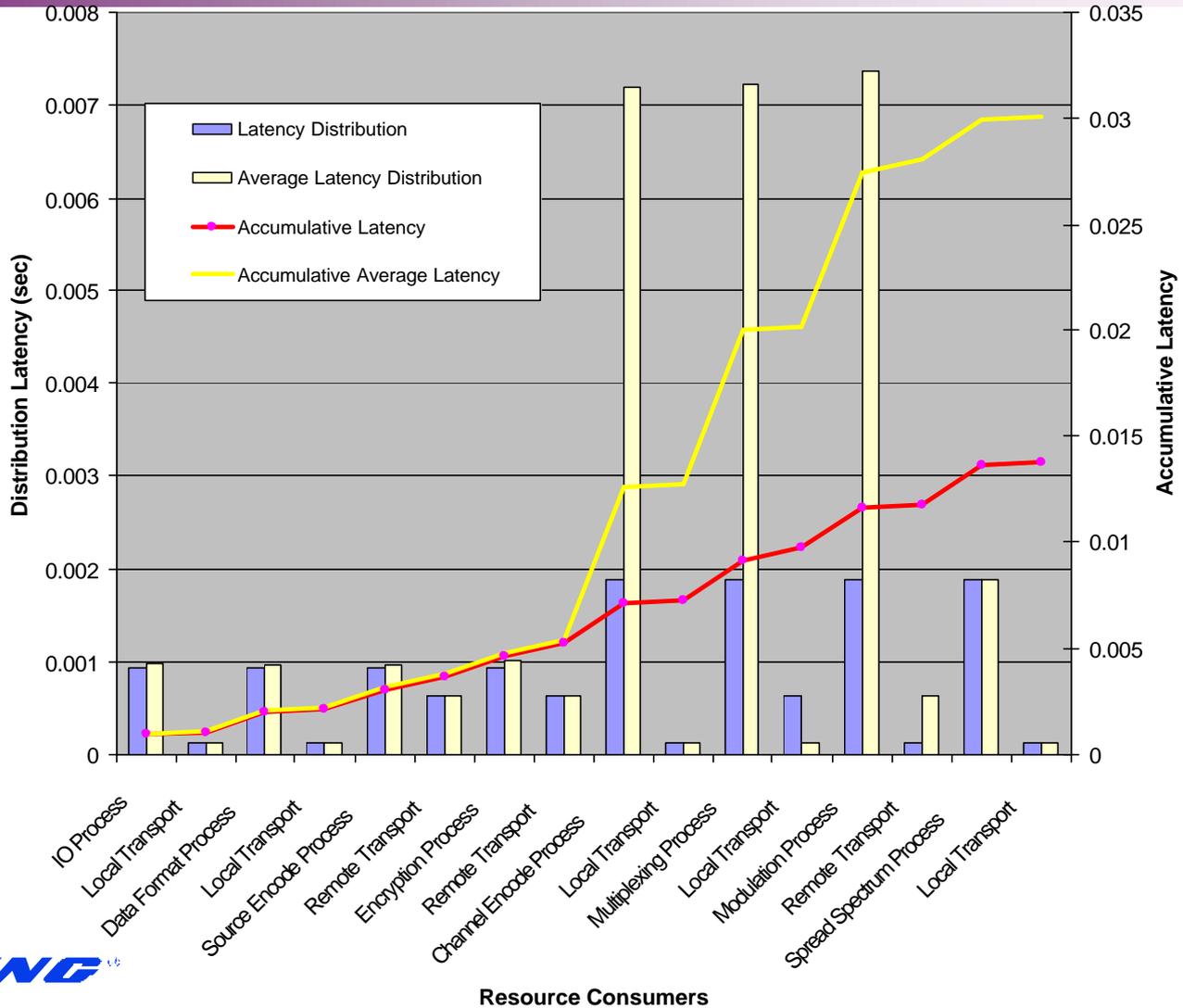
Scenario II – Latency

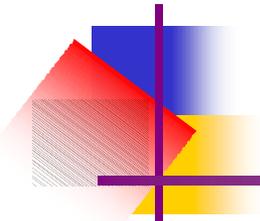


Scenario III – Resource Utilization



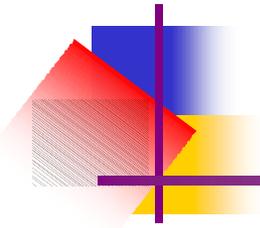
Scenario III – Latency





Conclusion

- Validated that hardware capability satisfied resources required by waveform software
- Validated that a waveform partitioned to match hardware resources, and maximized software portability and performance
- Co-design approach helps to optimize flexibility and performance
- It minimizes risks and maximizes chance of successful completion



Future Work

- Trade studies on
 - Message priority and length
 - Data throughput and latency
 - Component queue length
 - Probability distribution of data input/output