UML Profile for SDR Hardware/Software Adequacy Verification

Software-Based Communications (SBC) Workshop:
From Mobile to Agile Communications
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A3S RNRT project

Plan

- A3S project
- Profile Definition
  - QoS and Fault tolerance profile
  - PIM and PSM for software radio profile
- Profile use for software radio modeling
  - Hardware
  - Software
  - Deployment
- Verification process

The A3S project

- Adéquation Architecture - Application Système (A3S)
- French research program of collaborative projects - RNRT
- Funded by French Ministry of industry
- 2 years project - started in Sep. 2003
- Consortium
  - Thales
    - telecommunication system provider
  - Softeam
    - company, UML CAD tool provider - Objecteering
  - Lester, University of South Britanny
    - academic, SoC design tool, IP design
  - Mitsubishi Electric ITE
    - research lab, mobile and infrastructure manufacturer

The A3S goals

Performance prediction of a SDR system before effective implementation (at design phase)

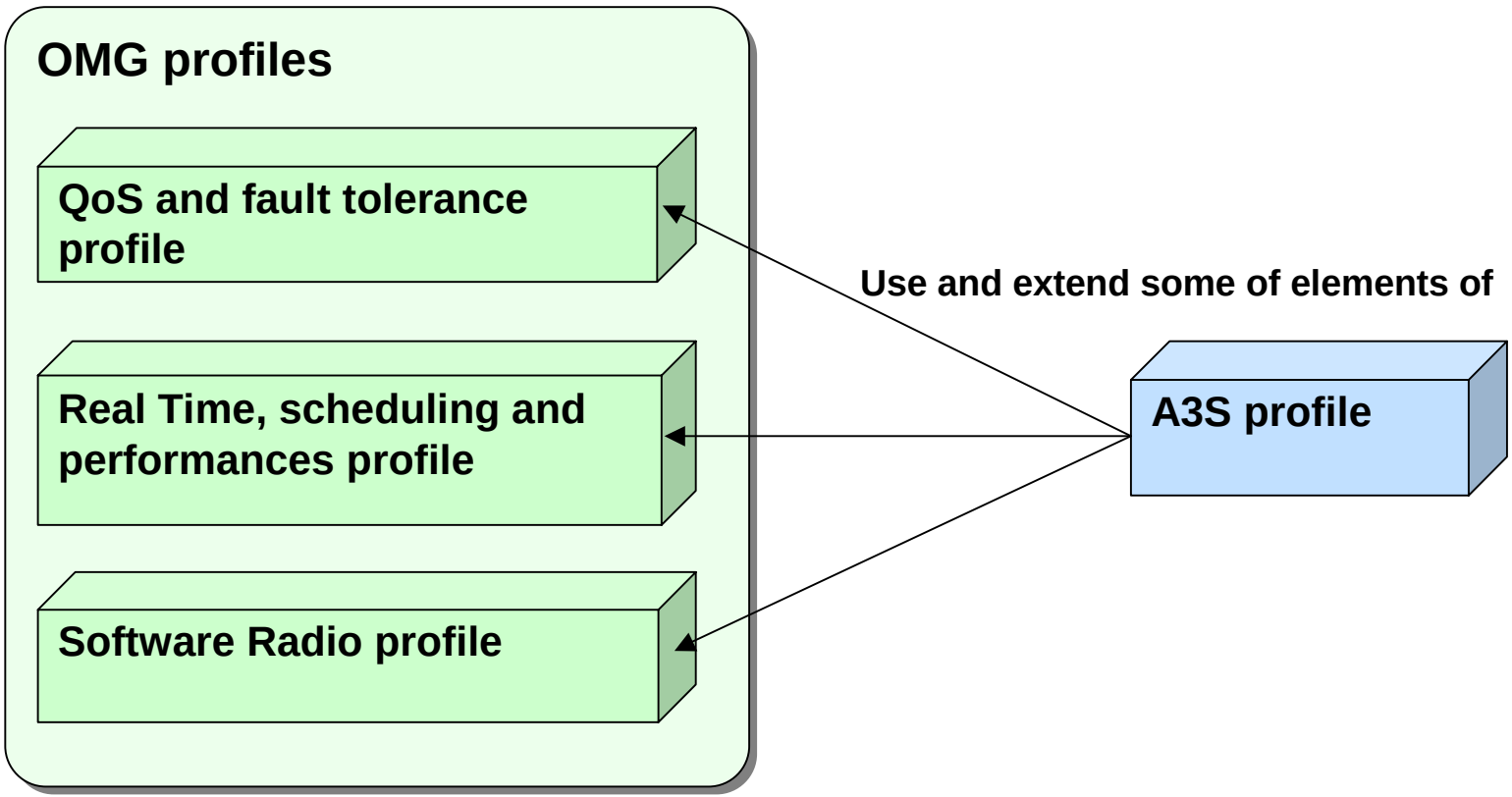
Methodological approach for SDR based on UML

- create an A3S profile for SDR physical layer representation
- UML tool support: Objecteering™ from Softeam
- UML description of
  - SW radio application
  - HW platform
- non functional characteristics and parameters collection

Processes behaviour verification engines (Lester)

- structural coherence verification
- execution model (period coherence, deadline, iteration number...)
- mapping coherence (enough memory resources)
- scheduling
- timing performance - memory use - FPGA use (max and trace)

Relation between OMG profiles and A3s profile

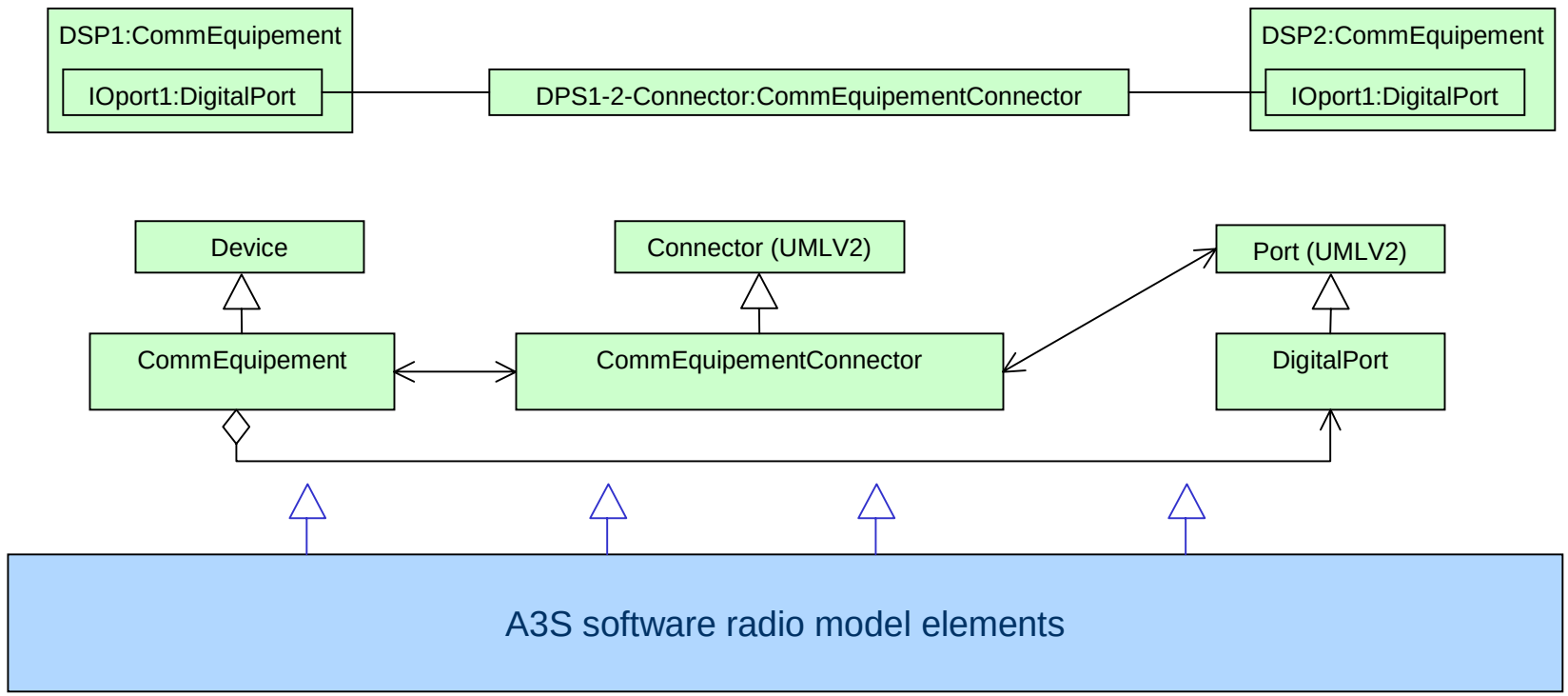


Use of the Software Radio profile

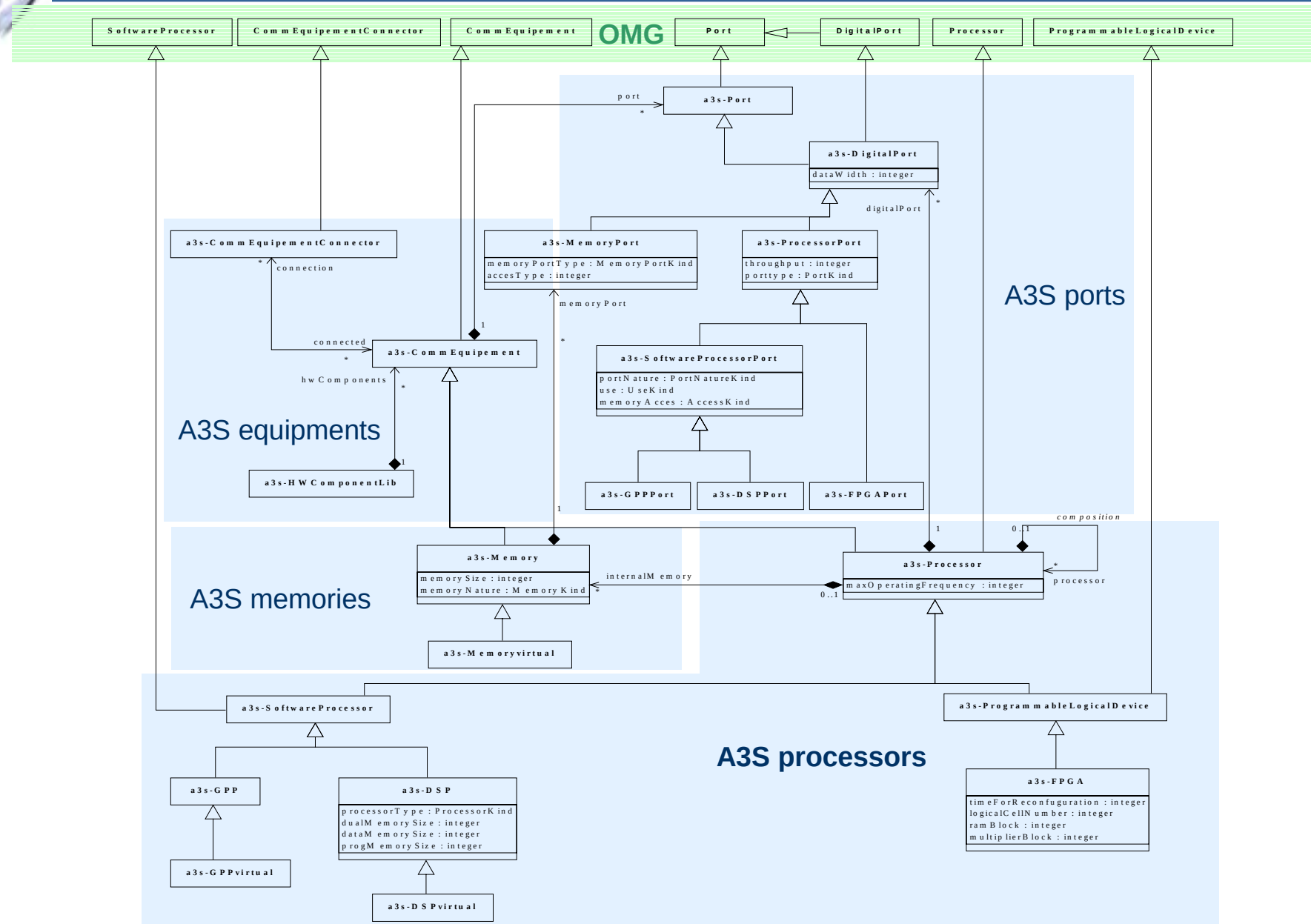
Hardware

- All hardware elements are **CommEquipement**
- They are communicating through **DigitalPort**
- DigitalPort are connected through **CommEquipementConnector**

- **A3S inherits from these elements**



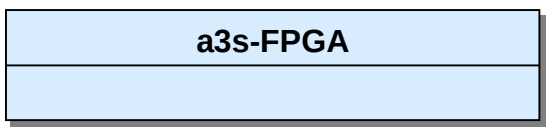
PIM Hardware meta-model

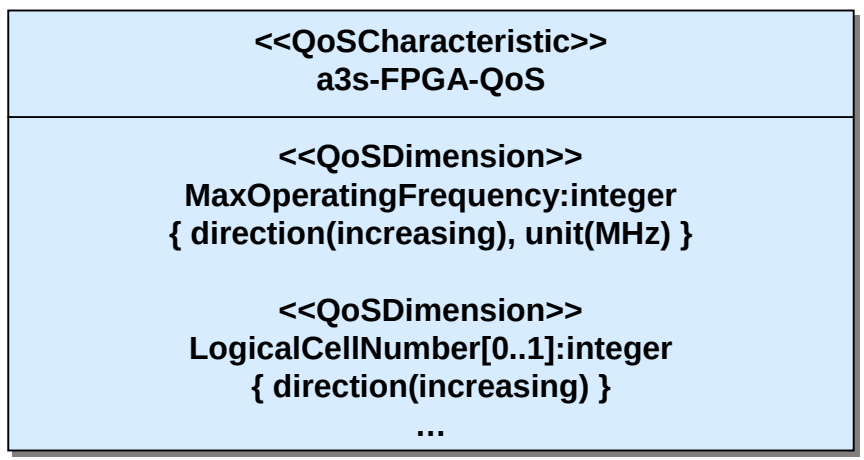


Use of the QoS and Fault Tolerance Profile

- Definition of the QoS language which will be used in the model
  - ➔ Creation of a set of QoSCharacteristics dedicated to the A3S usage
    - mostly reuse QoSCharacteristic already defined in the QoSprofile
    - definition of new QoSCharacteristics
    - possibilty of inheritance and aggregation of QoSCharacteristics

- Assembly of QoS Characteristics will be grouped in a A3S QoSCatalog representing the QoS language.
- Each A3S stereotype will be associated to a specific QoSCharacteristic



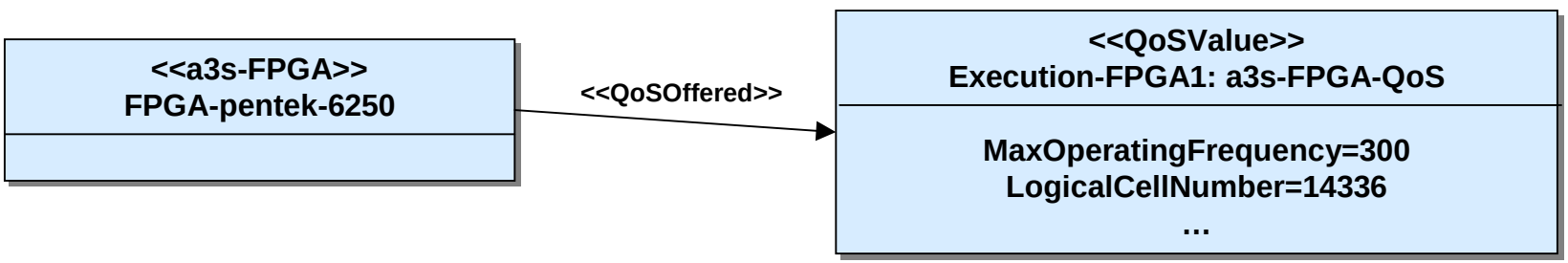


Use of the QoS language, first method

- QoS language (PIM) will be used to specify the QoS of PSM radio elements.

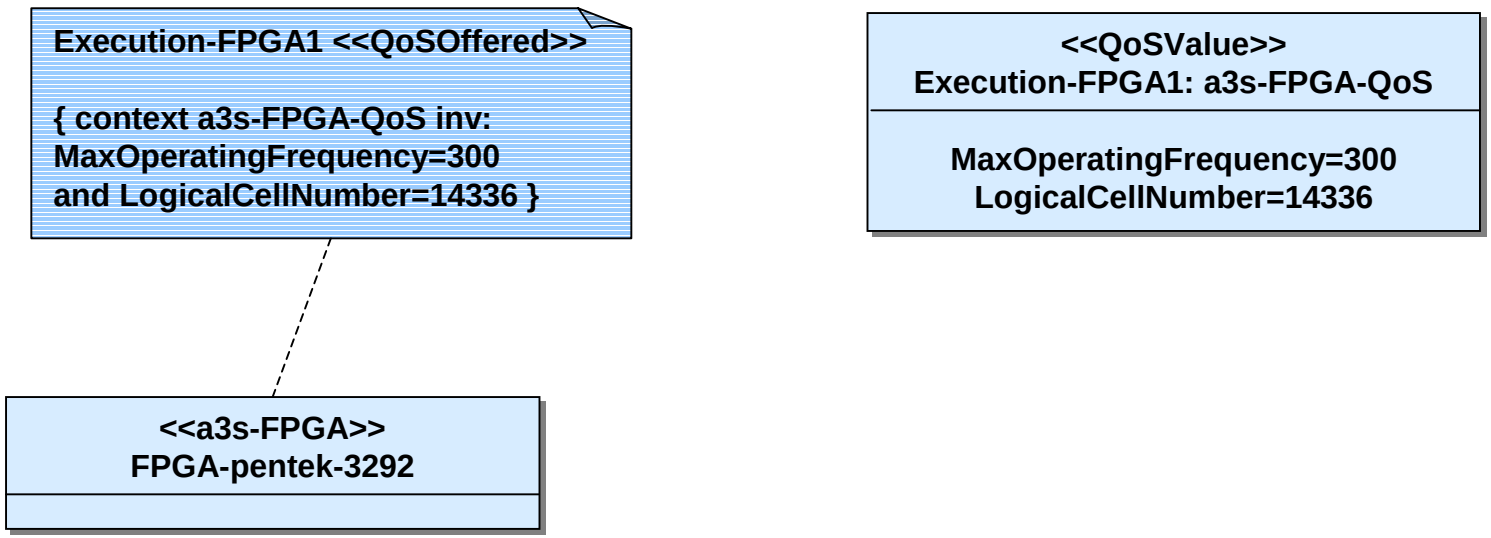
PIM	PSM
A3S PIM elements (ex: FPGA)	A3S PSM elements (ex: FPGA-pentek-3292)
QoSCharacteristic	QoSValue

- QoS stereotypes on dependencies decribe how the QoS is applied



Use of the QoS language, second method

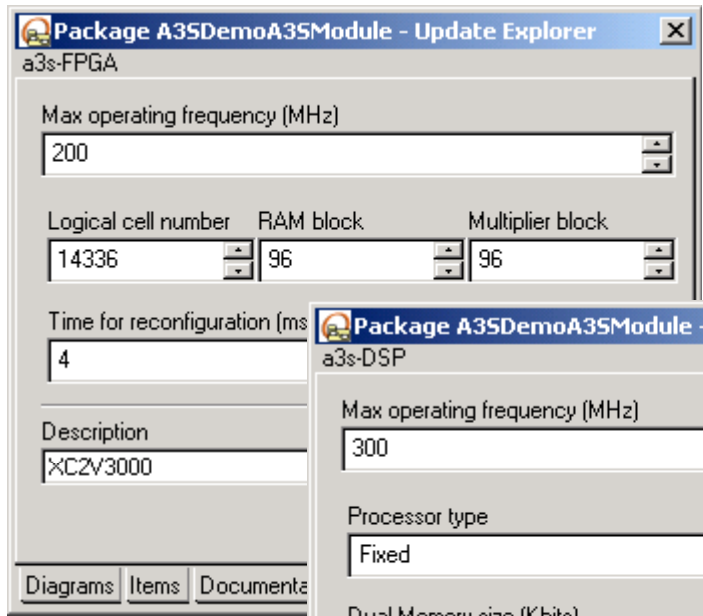
- More commonly used method
- Use of a context to specify how the QoS is applied
- logical operator for fine granularity QoS definition



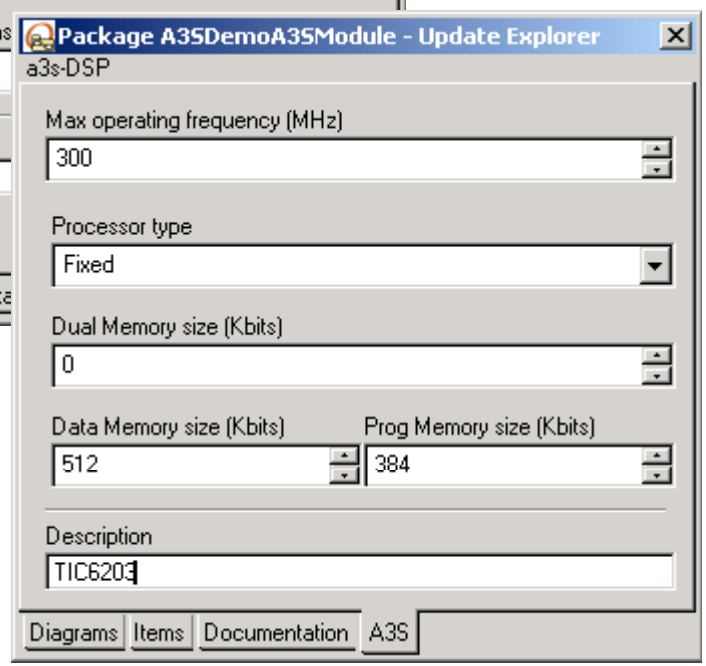
QoS through user friendly interface

- User Friendly interface
- Fully integrated to the UML tool
- Specific to the A3S element
  - FPGA
  - DSP
  - FIFO
  - …
- Allow in-design verification
  - Checklist
  - calculation
  - combination

for a FPGA Xilinx XC2V3000



for a TIC6203 DSP

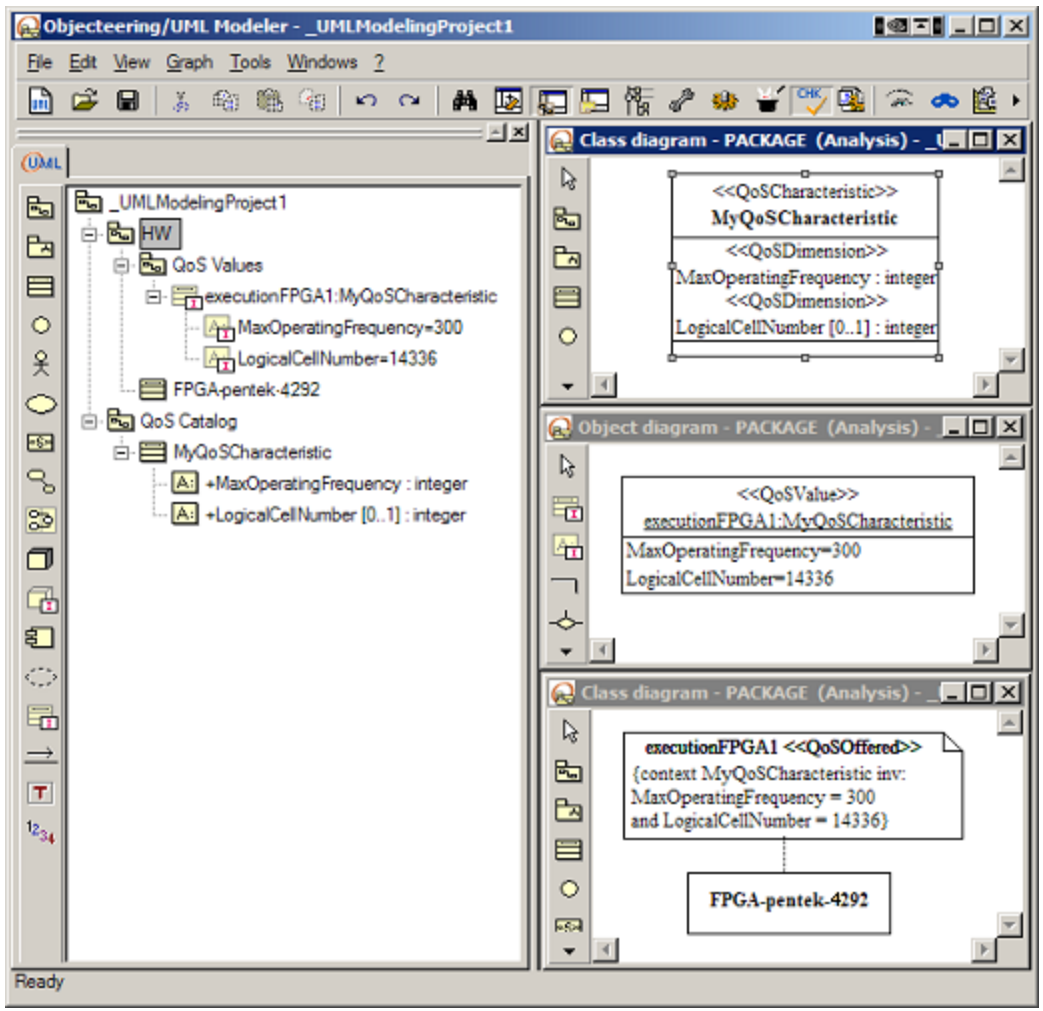


- Translation user interface ➔ UML classes

- Time saving for A3S model elaboration

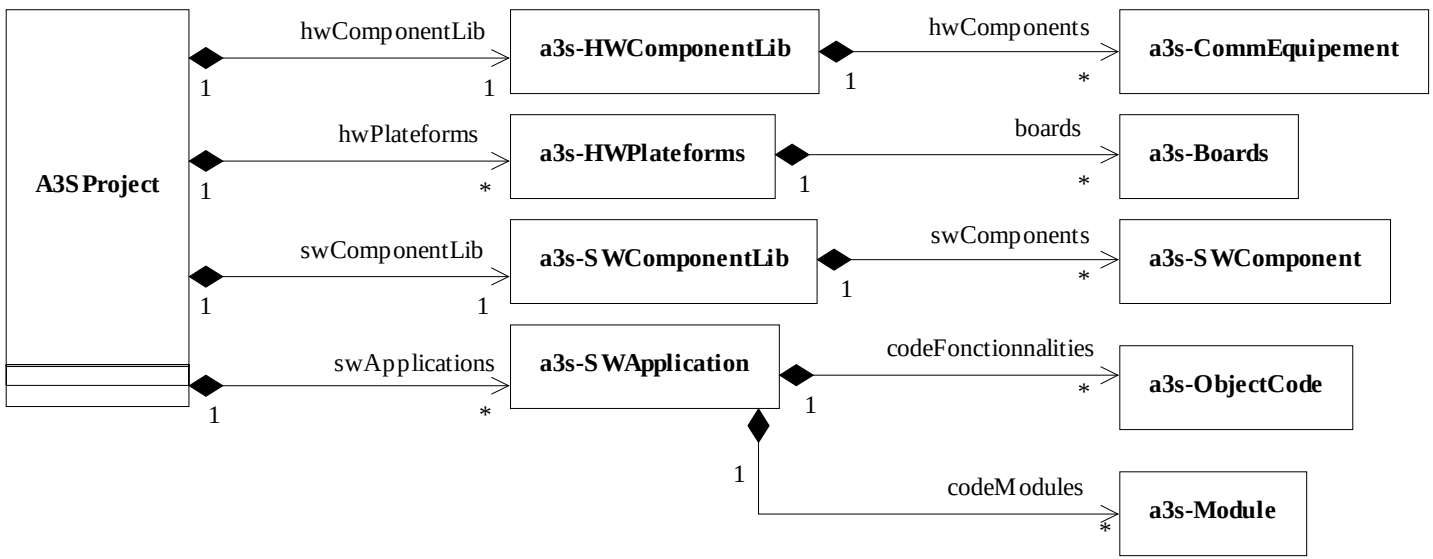
Use of the QoS profile, UML tool

- Example of the result of the user input



Library approach

- UML design
  - Hardware components
  - Software components
  - Hardware platform
  - Software platform
- Advantages
  - Importation
  - 3rd party
  - Components catalogue
  - Extendable



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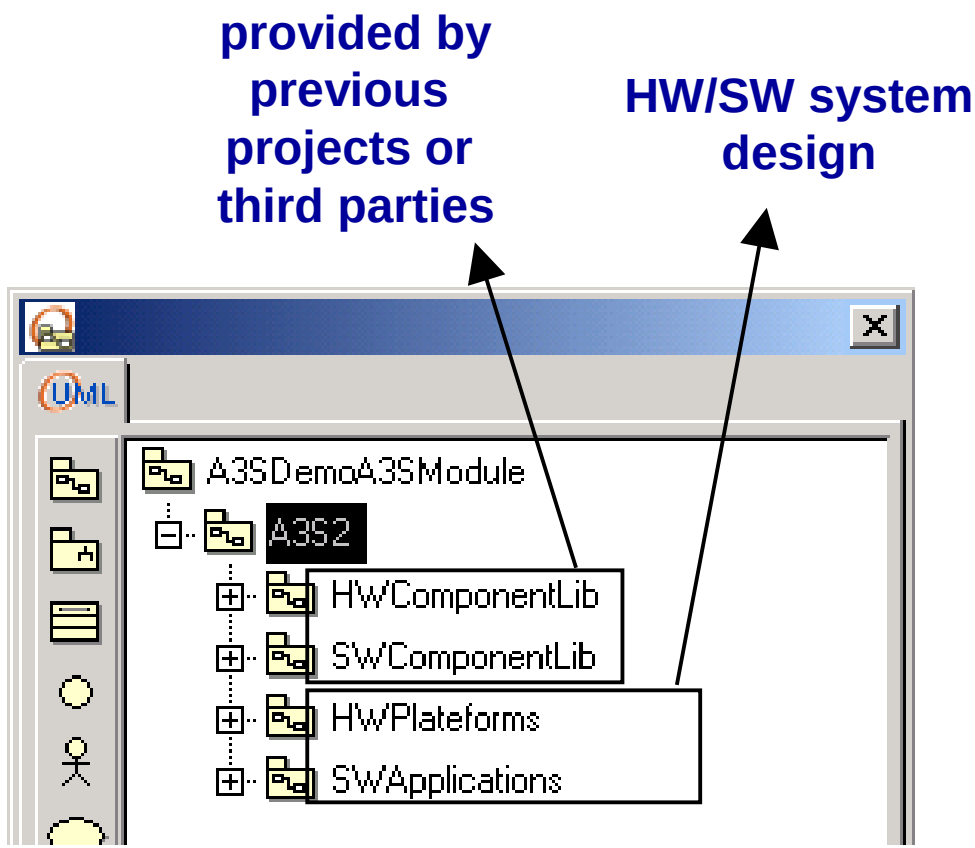
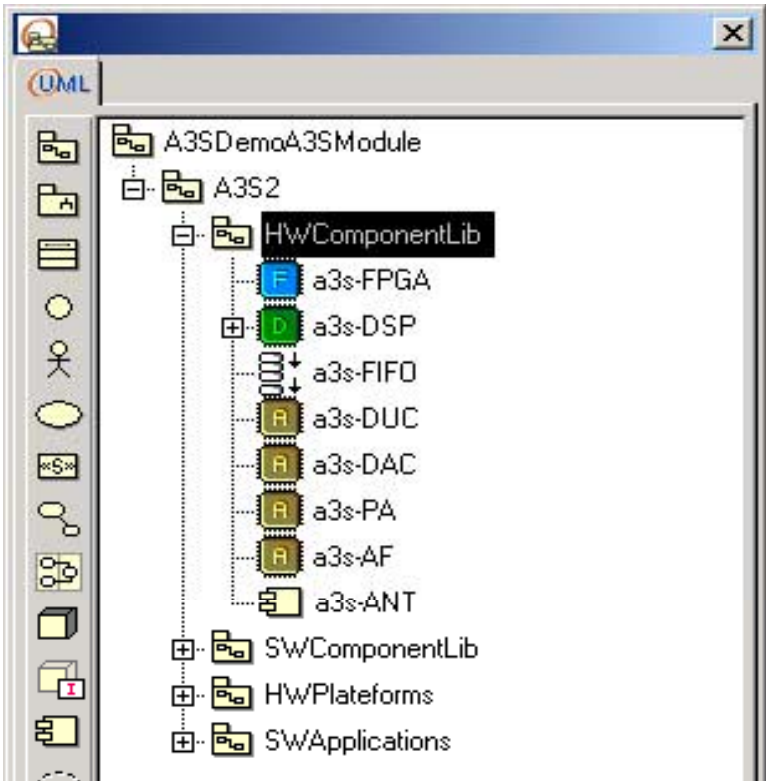
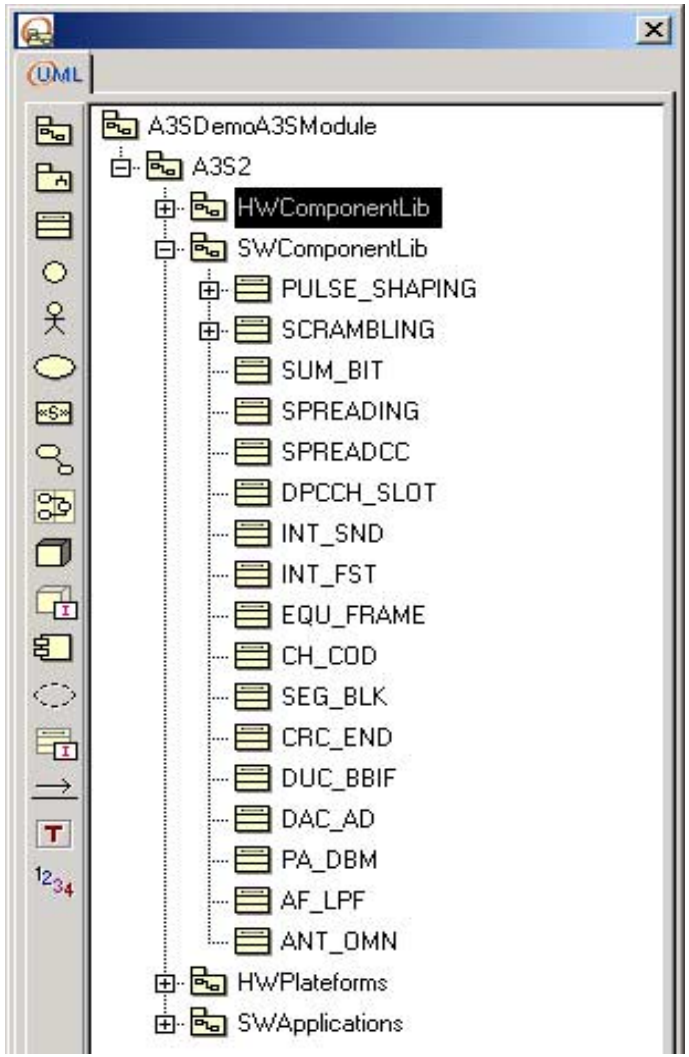


Library approach

Hardware

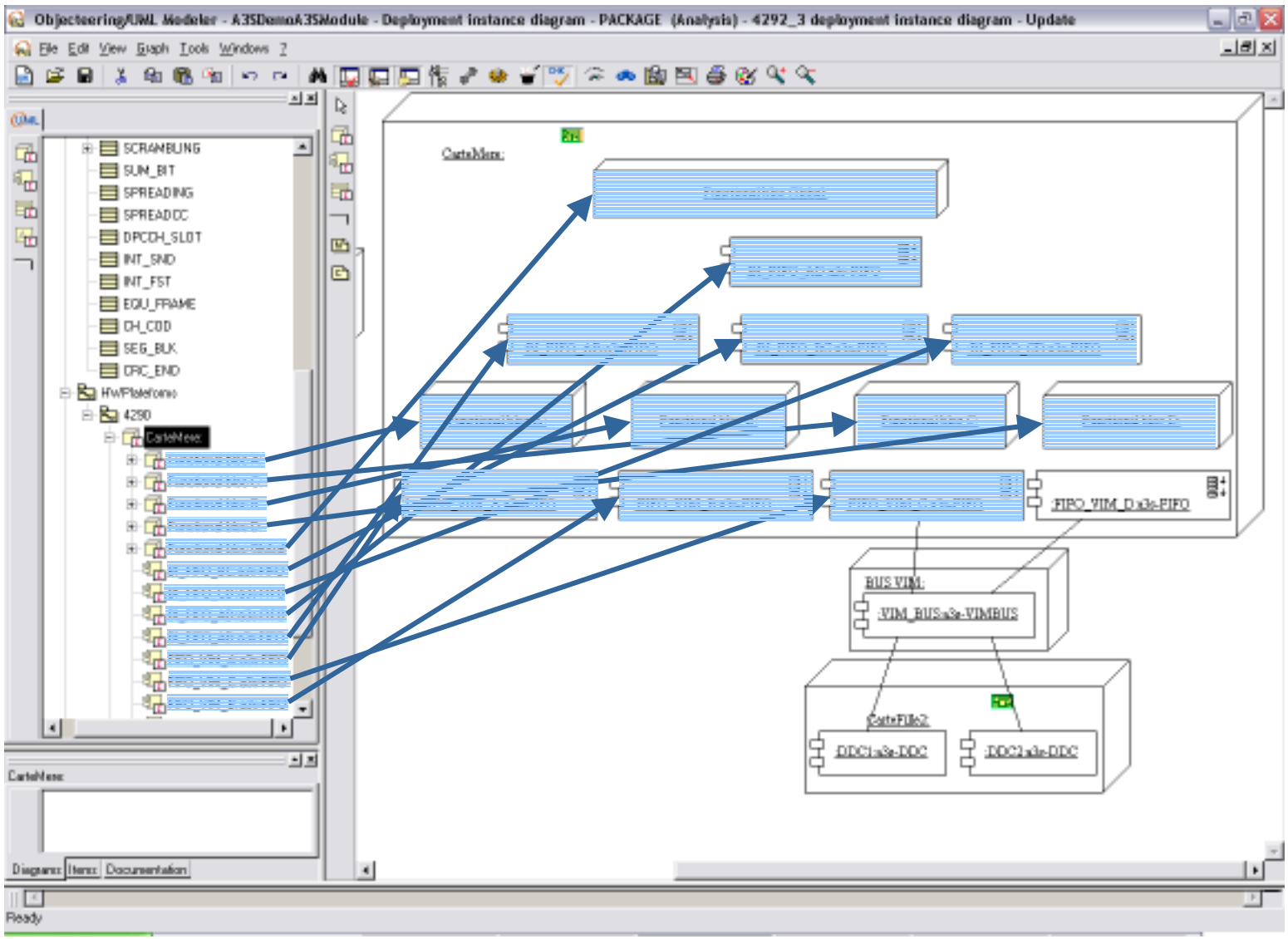


Software

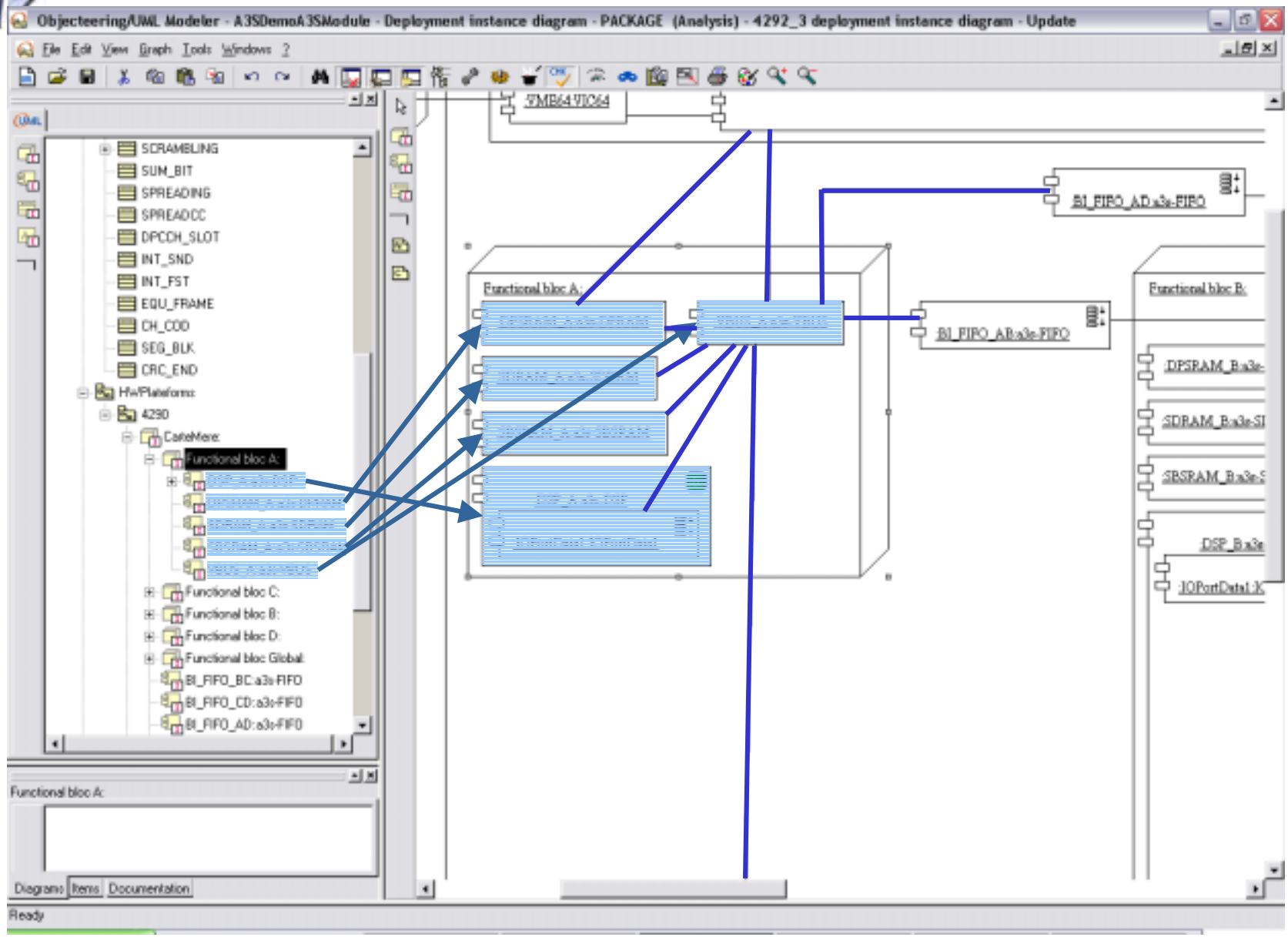


+ Associated characteristics

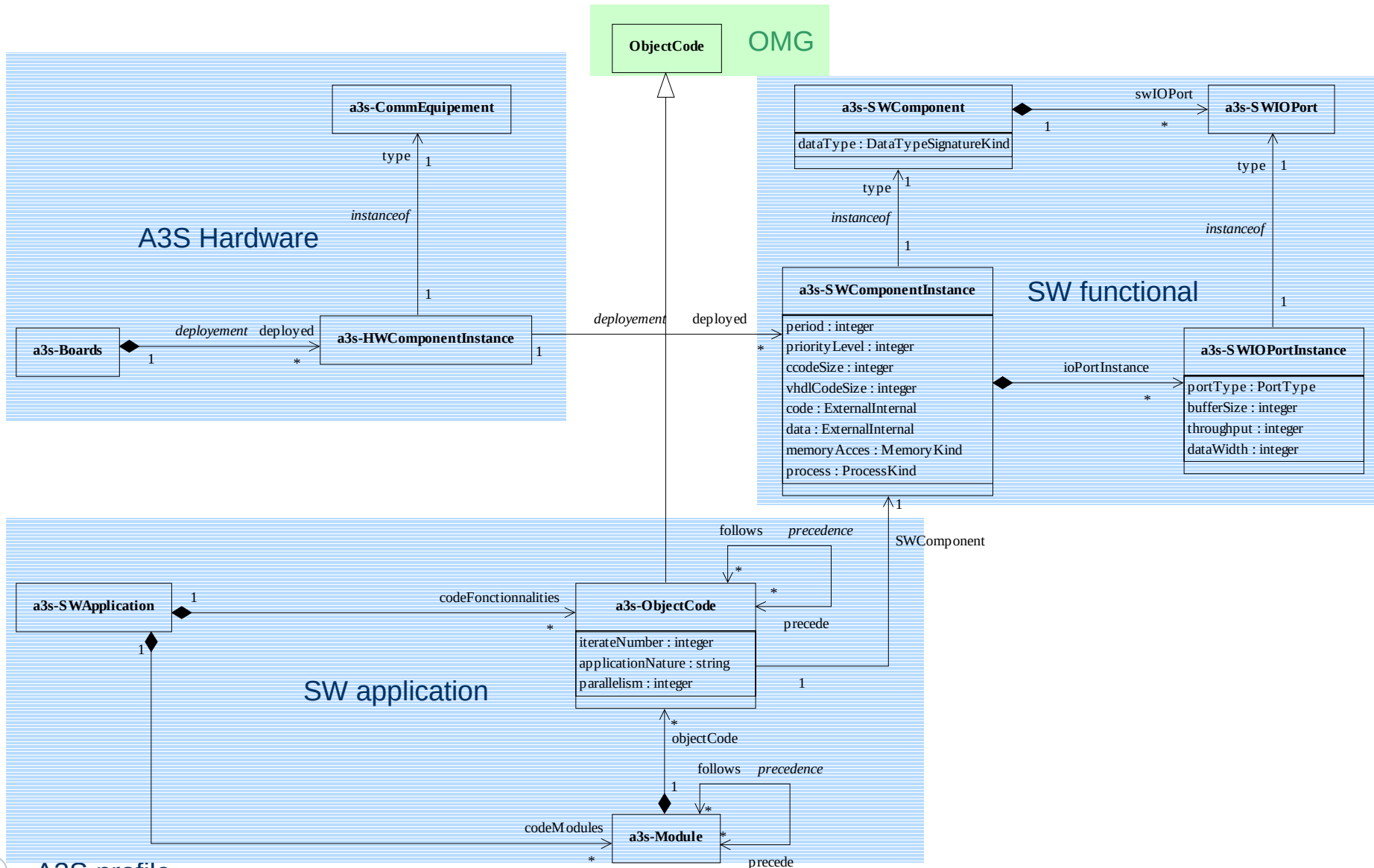
Hardware platform design 1/2



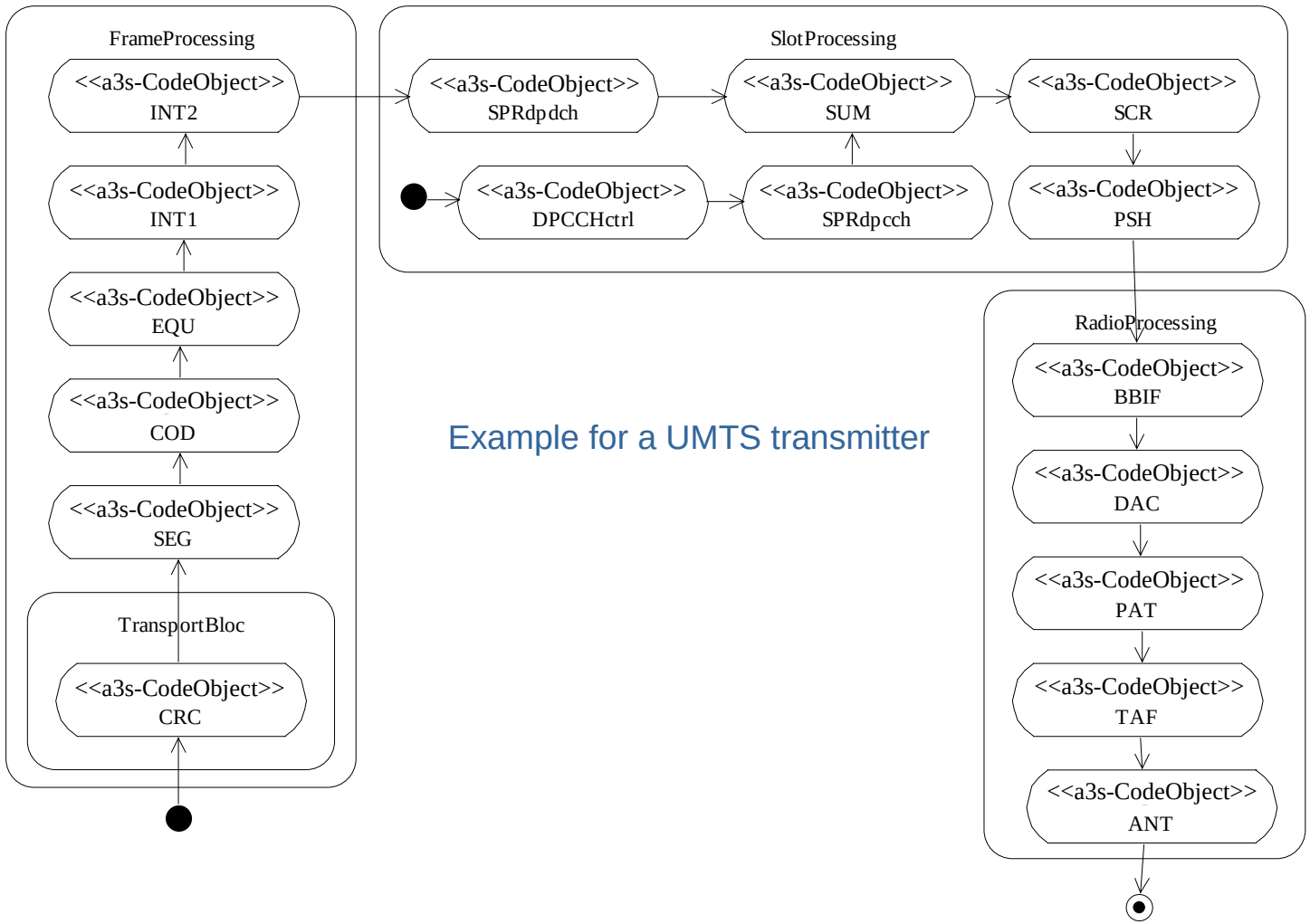
Hardware platform design 2/2



Deployment meta-model



- An activity graph is used in order to design the Waveform functional aspect



Example for a UMTS transmitter

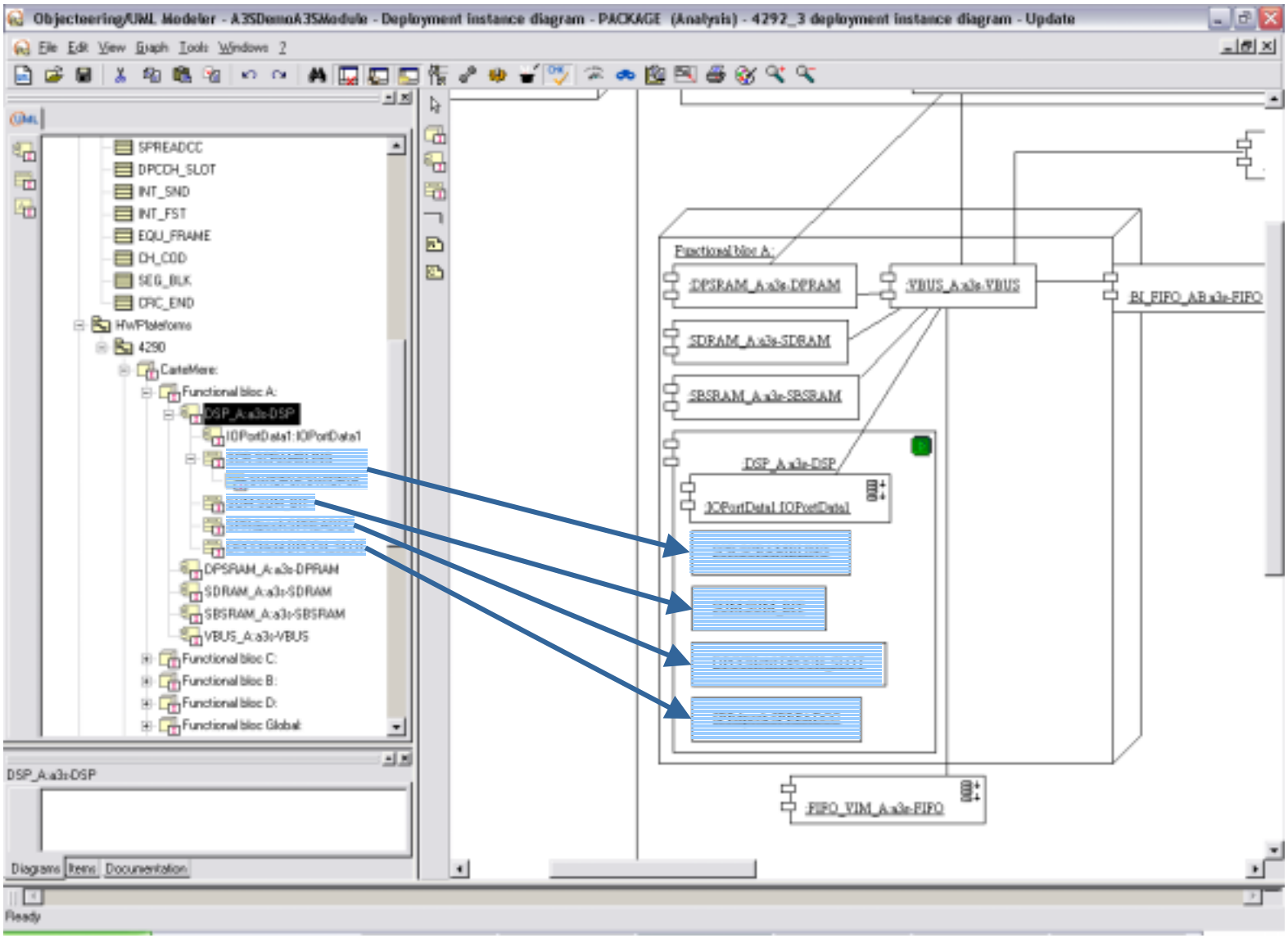
Use of the QoS profile in software design

- There may be several iterations per a3s-operation.
- Each iteration can be processed on a specific a3s-processor

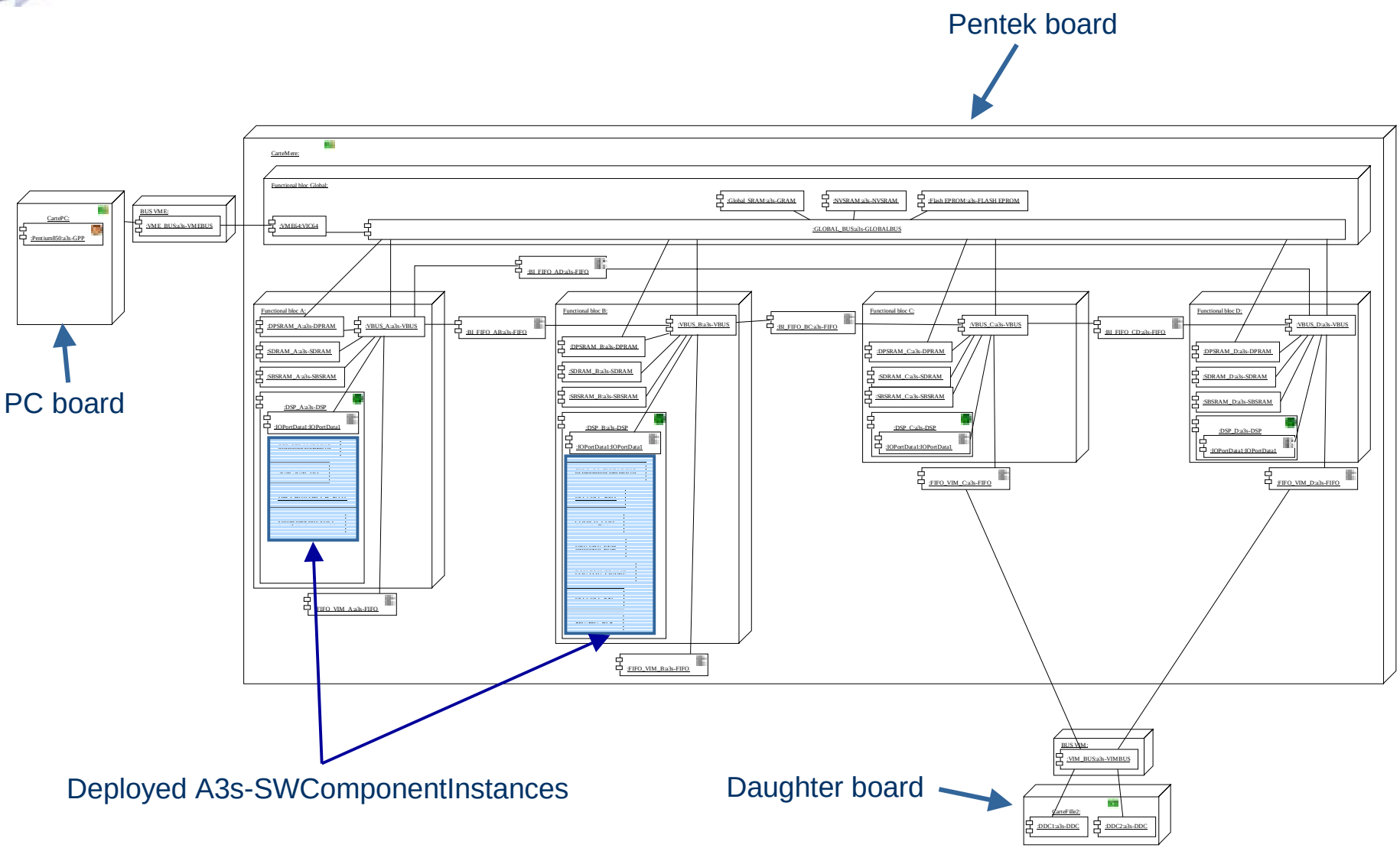
- So
  - Each a3s-operation is linked to an QoS-Characteristic
  - Each iteration of an a3s-operation is categorized by a QoSValue

Software functional deployment

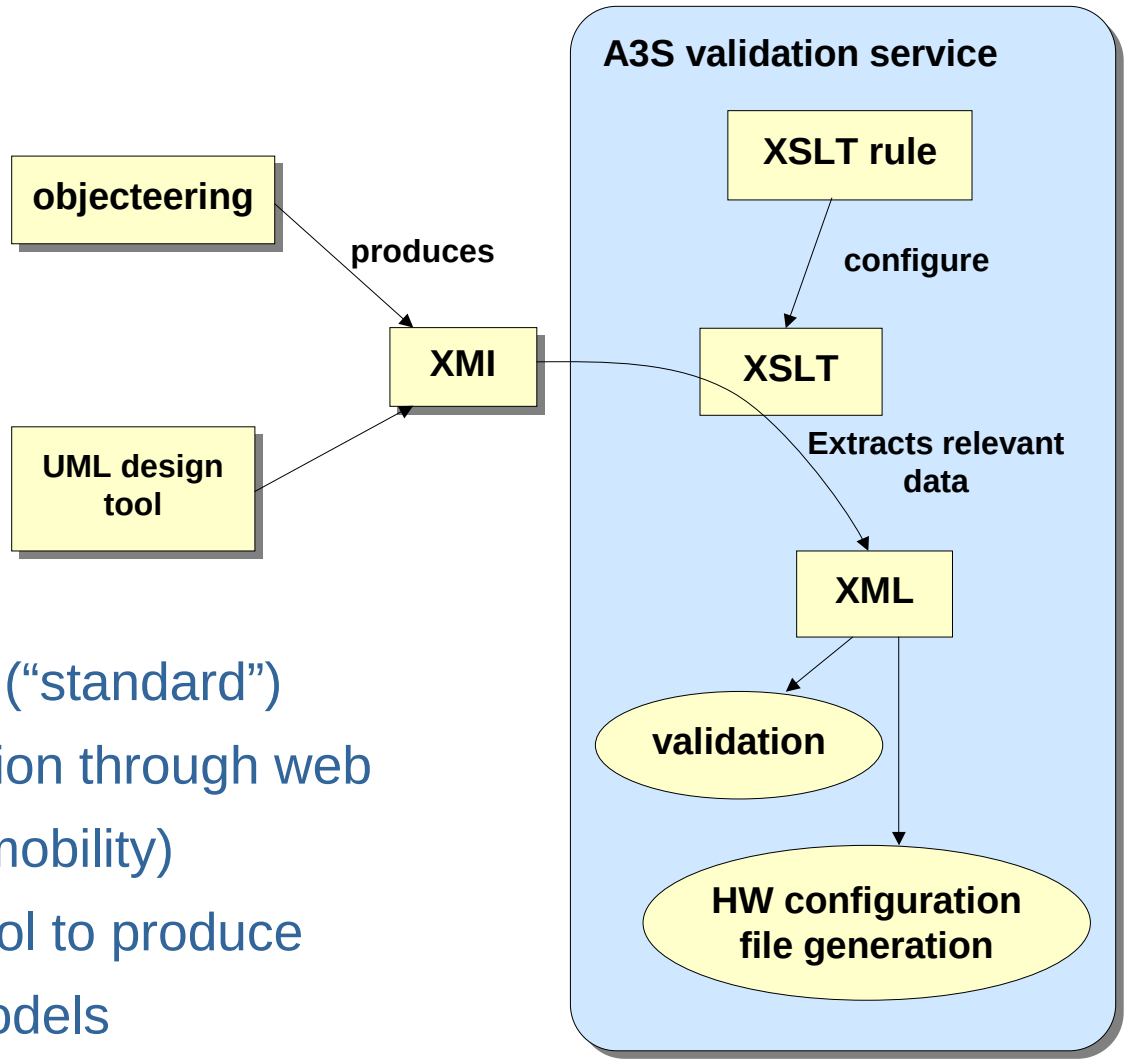
Placement of functional elements on Hardware Architecture



Deployement, general view



Service validation process



- XMI ➔ “portability” (“standard”)
- Service ➔ verification through web

(verify anywhere ➔ mobility)

- Allow other UML tool to produce

A3S verifiable models

Next improvements

- Use of QoS and Fault Tolerance profile elements in software design
- Automatic translation of Software iteration from user interface informations to UML elements
- Use of Real Time scheduling and performances elements

(sequence diagrams for timing visualisation ?)

Many thanks for your attention.

Questions ?

THALES

SOFTEAM
Think Object

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