Efforts to Implement an SCA Compliant Wideband MILSATCOM Waveform

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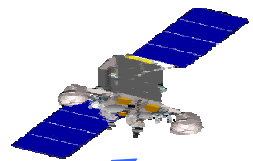
The Case for SDR

- Commercial-based approach implemented world-wide
  - Vast industry and government investment
- Inherent product line features
  - Architecture-centric, scaleable, extensible, reusable components
- Established architecture framework (SCA) provides low risk
- Designed for technology insertion
  - New waveform software applications, tracks Moore's law
- Low total system ownership cost
  - Software applications, COTS-based components, reusable components

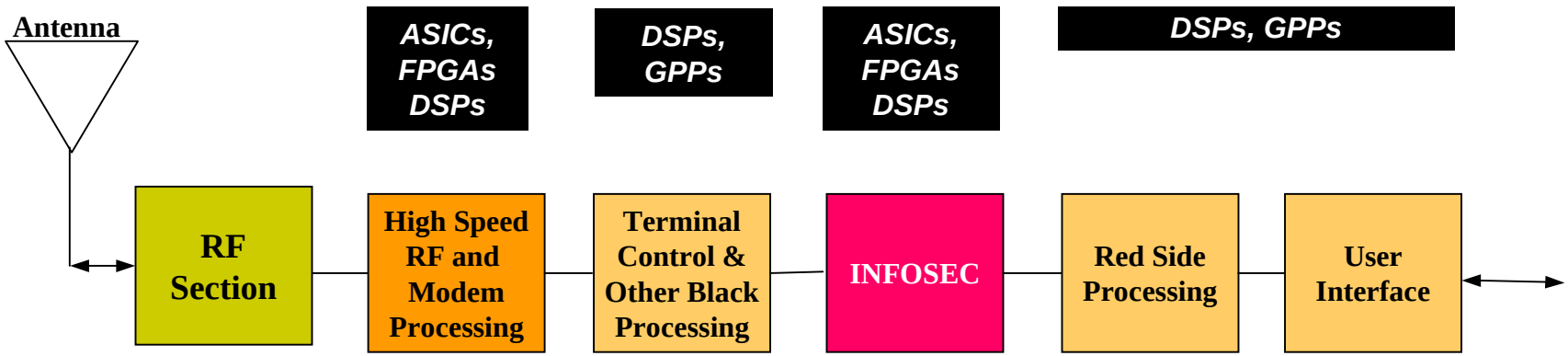
Why SDR Technology for MILSATCOM Terminals?

- Software Defined Radio (SDR) technology and a product line architecture approach provide for increased flexibility, interoperability, and reduced overall costs to DoD
  - Enhances terminal reconfiguration capabilities
  - Easier to add new waveforms to terminals
  - Allows for third party development
    - Better products, more cost effective
  - Develop waveforms once and port to other terminals
    - Reduces development and maintenance costs
    - Reduces time and cost to achieve interoperability



PRODUCT LINE OF TERMINALS BASED ON COMMON ARCHITECTURE

Generic View of a MILSATCOM Terminal -- Questions Related to Use of SCA



- **What waveform application features and implementations can be used to form the "base" for above 2 GHz SATCOM waveforms?**
- **What dynamic reconfiguration and QoS features can be applied for Specialized Hardware?**
- **How much code will be portable between processing elements (e.g., DSP to GPP, FPGA to DSP, FPGA to FPGA)?**
- **What part of the waveform will NOT be "portable"?**
- **What are the implications of real-time processing (e.g., predictable timing, latency, CPU and memory utilization)?**

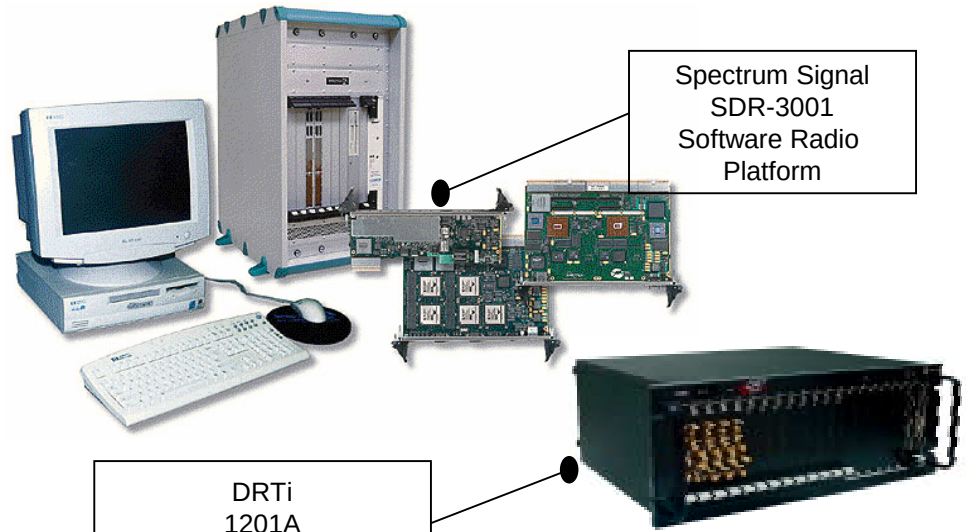
SCA for Above 2GHz Waveforms

ISSUE

What are the technical challenges associated with making above 2GHz MILSATCOM terminals SCA compliant so that DoD can implement an optimum number of Programs?

BACKGROUND

- **JTRS is the DoD overarching program to leverage SDR technology and develop a "family" of software re-programmable radios**
- **The initial spectrum range (2MHz-to-2GHz) was chosen partially because of limitations in RF and processor technology**
- **A MITRE led study concluded in 2003 that advances in RF and processor technology were such that DoD *can* attain the benefits of software radio technology for their MILSATCOM terminals**
- **OSD ASN (NII) issued a modification (17 Jun 03) to the Radio Acquisition Policy (28 Aug 98) which states "…that all…systems, including those operating above 2GHz, are required to be developed in compliance with JTRS/SCA"**
- **There is a need to explore potential alternatives for implementing JTRS for DoD communication systems that operate above 2GHz**



LAB ACTIVITIES

- **Implement a representative above 2GHz waveform on an SCA compliant communications platform**
- **Prototype SCA extensions required for Above 2 GHz MILSATCOM terminals (in accordance with JTRS JPO releases of the SCA specification)**
- **Perform experiments/tests designed to advance understanding of SCA extensions (e.g., validate proposed extensions to SCA standard)**
- **Publish results of experiments and, as appropriate, collaborate with JTRS JPO on SCA extensions**

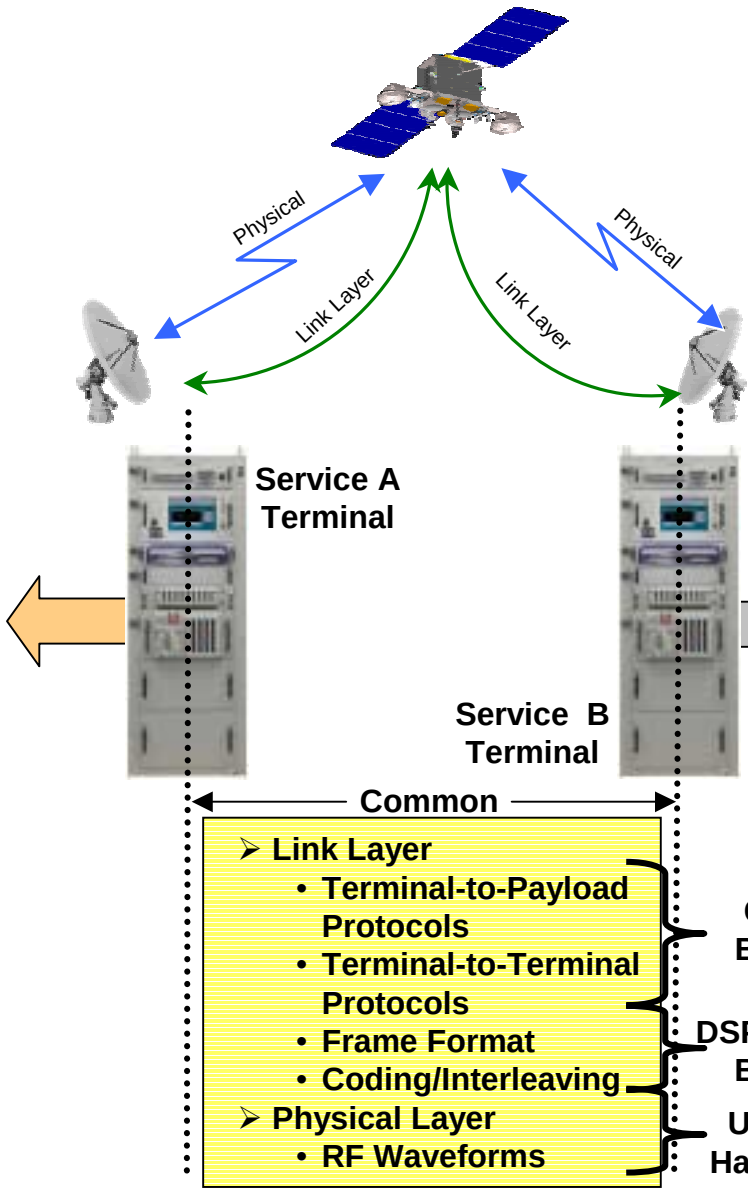
Some Major Issues to be Addressed

- For SCA-based MILSATCOM waveforms, what would be the degree of waveform application portability and software reuse?
  - MILSATCOM wideband terminal RF section and modem processing require special purpose hardware (e.g., FPGAs)
    - As data rates increase into the 10s and 100s of Mbps, computational load will outpace future DSP and GPP trends – ASICs and FPGAs will be needed
  - Wideband SATCOM “waveform” implementation will have to be distributed among various specialized hardware components (FPGAs, ASICs) and software modules
    - Interfaces among the various components will need to be defined
    - SCA 3.0 supplement needs to be implemented for specialized hardware
  - Porting of MILSATCOM waveforms is difficult because of the mix of processing hardware (GPPs, DSPs, FPGAs, and ASICs), software “modules” (e.g., C, C++, VHDL), and interconnect technologies (e.g., CORBA, HAL-C)
- What are the implications of real-time processing (e.g., predictable timing, latency, CPU and memory utilization)?

Overview of MILSATCOM Waveforms Above 2 GHz

	Purpose	Waveform Designation	Modulation	MA scheme	Data Rates (Mb/s)	Frequency Bands (GHz)	MILSATCOM System
Protected	• Provides assured and survivable communications for strategic military operations • Resists jamming and nuclear scintillation	LDR	FSK, DPSK	FH-FDM/TDMA	<< 0.1	44 (uplink) 20 (downlink)	Milstar, UFO-E & AEHF
		MDR	DPSK	FH-FDM/ TDM	< 1.5		
		XDR	FSK, DPSK, GMSK	FH-FDM/ TDMA	< 8		AEHF & T-SAT
		XDR+	TBD	FH-FDM/ TDMA	< 45		T-SAT & APS
Wideband	• Supports entire spectrum of tactical military operations from major theater war to humanitarian assistance	X-band waveforms	BPSK, (O)QPSK & 8-PSK 16-QAM	FDMA, SSMA	< 20	8 (uplink) 7 (downlink)	DSCS & WGS
		Ka-band waveforms	BPSK, (O)QPSK, 8-PSK & 16-QAM	FDMA	< 155	30 (uplink) 20 (downlink)	WGS
		Ka- and Ku band waveforms	QPSK	Broadcast	12 – 48	30/14 (uplink) 20/12 (downlink)	GBS (rcv only on UFO 8, 9, 10)/ multiple comm'l
		Commercial transponded	n-PSK	FDMA	Varies	C, Ku	Varies
Laser	• Backbone connectivity for TC • High band video and imagery data	Laser	TBD	TBD	> 1,000	Optical	T-SAT

Problem Characterization



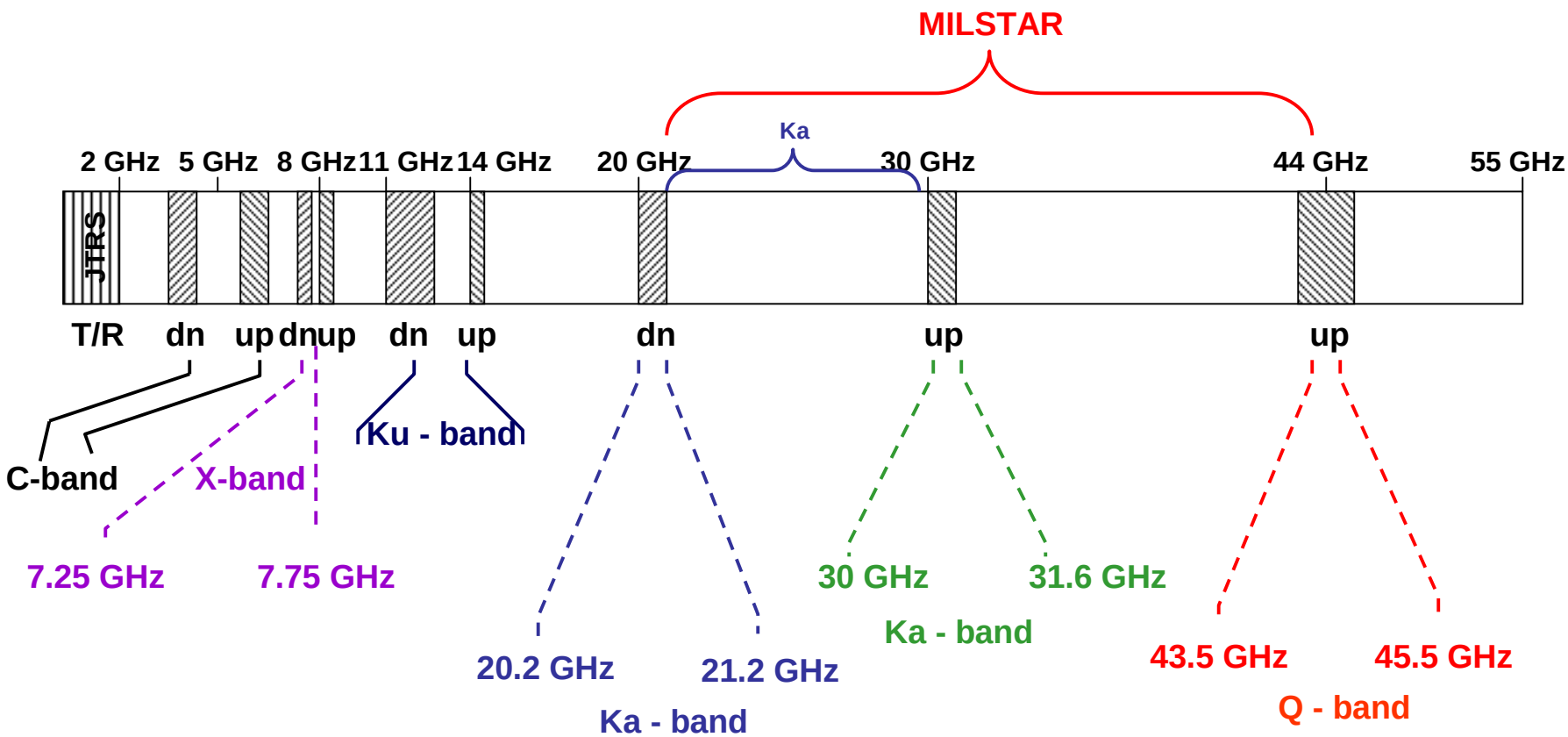
- External Controls, Components and Interfaces
  - Antennas for A
  - Support Systems for A
  - Baseband for A (some are common)
  - User Interface for A
  - Frequency Plan
- Internal Processing
  - Algorithms for A
  - Link Layer Processing for A (some are common)
    - Access Control Protocols
    - Resource Management
  - Physical Layer for A
    - Demodulation
    - Soft Decision Levels

Service A Unique

- External Controls, Components and Interfaces
  - Antennas for B
  - Support Systems for B
  - Baseband for B (some are common)
  - User Interface for B
  - Frequency Plan
- Internal Processing
  - Algorithms for B
  - Link Layer Processing for B (some are common)
    - Access Control Protocols
    - Resource Management
  - Physical Layer for B
    - Demodulation
    - Soft Decision Levels

Service B Unique

SATCOM Frequencies



- **MILSATCOM bandwidths cover only 11% of the overall 2 GHz to 55 GHz bandwidth**
- **It is not cost effective for the terminal to cover this entire frequency range**

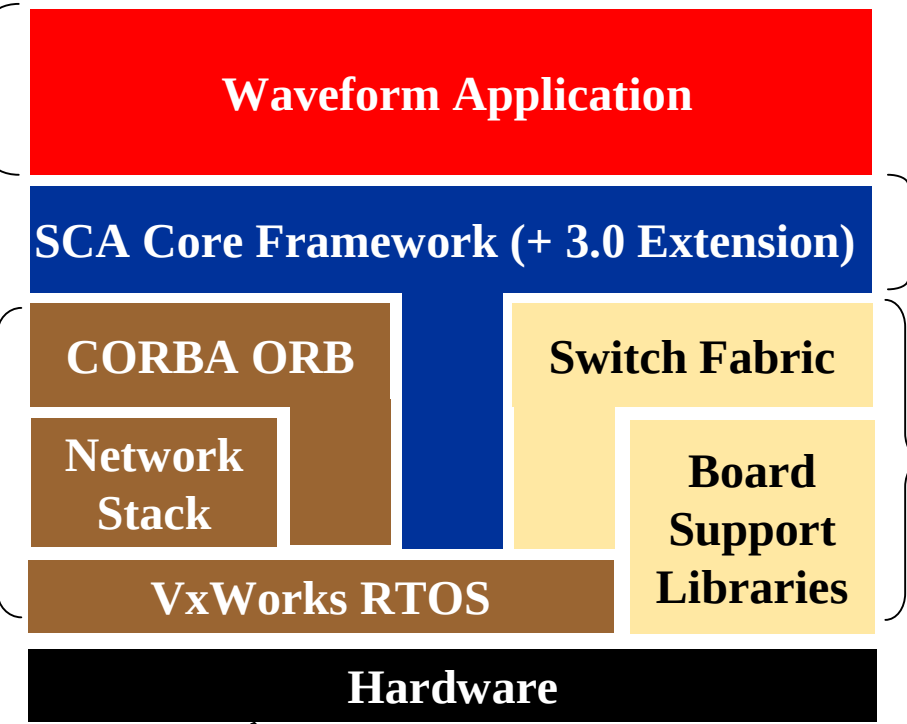
Evolving From Different Service Terminals

- Operational impacts on terminal design:
  - Hardware platform
    - Vibration, shock, platform location and associated environmental needs
  - Operator Interface
    - Functions executed by the terminal
  - Classification level of terminal
    - Operational uses cannot all support classified terminal implementation
  - Support system interfaces are different based upon installation platform
  - Antenna subsystem and associated control
    - Use of or lack of use of downlink signal to support antenna pointing
  - Terminal to platform interface
    - Ship, sub, shore, aircraft, transportable, man-portable

Services still need to develop "some" Service-unique attributes of terminals to meet operational needs of designated installation platforms

Overview of Implementation Approach

Above 2 GHz waveform that is representative of existing military systems



Spectrum Signal Processing SCA Core Framework + SCA 3.0 extensions (new dev)

Standards-Based COTS Software

Spectrum Signal Processing QuicComm switch fabric software and associated hardware support libraries

Implementation approach is to use commercially available SDR platform (SCA 2.2) and extend it to create an SCA 3.0 compliant waveform

Spectrum Signal Processing SDR-3100 Software Radio Platform

Experimental Waveform Objectives

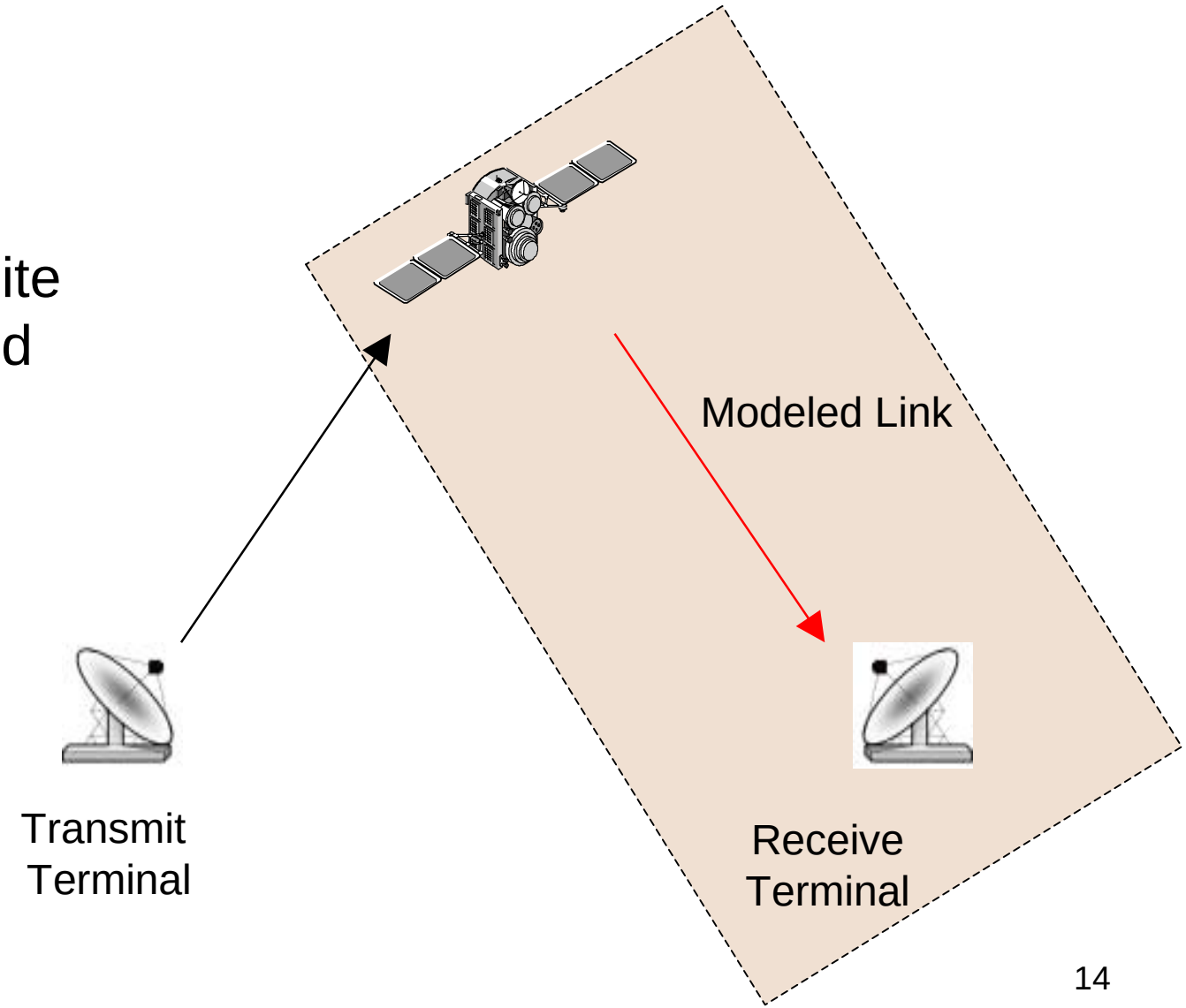
- Examine the options and issues related to implementing high bandwidth / high speed SCA compliant waveforms
- Develop a high bandwidth waveform that is representative of existing military systems
- Simplify where necessary
  - Ease hardware and software implementation as necessary
  - Keep only complexity necessary to exercise system and SCA
  - Ensure waveform is functional and representative
- Design in parameterization and flexibility to allow future waveform expansion as needed
  - For example, could add timing acquisition or access control messaging

Experimental Waveform Basics

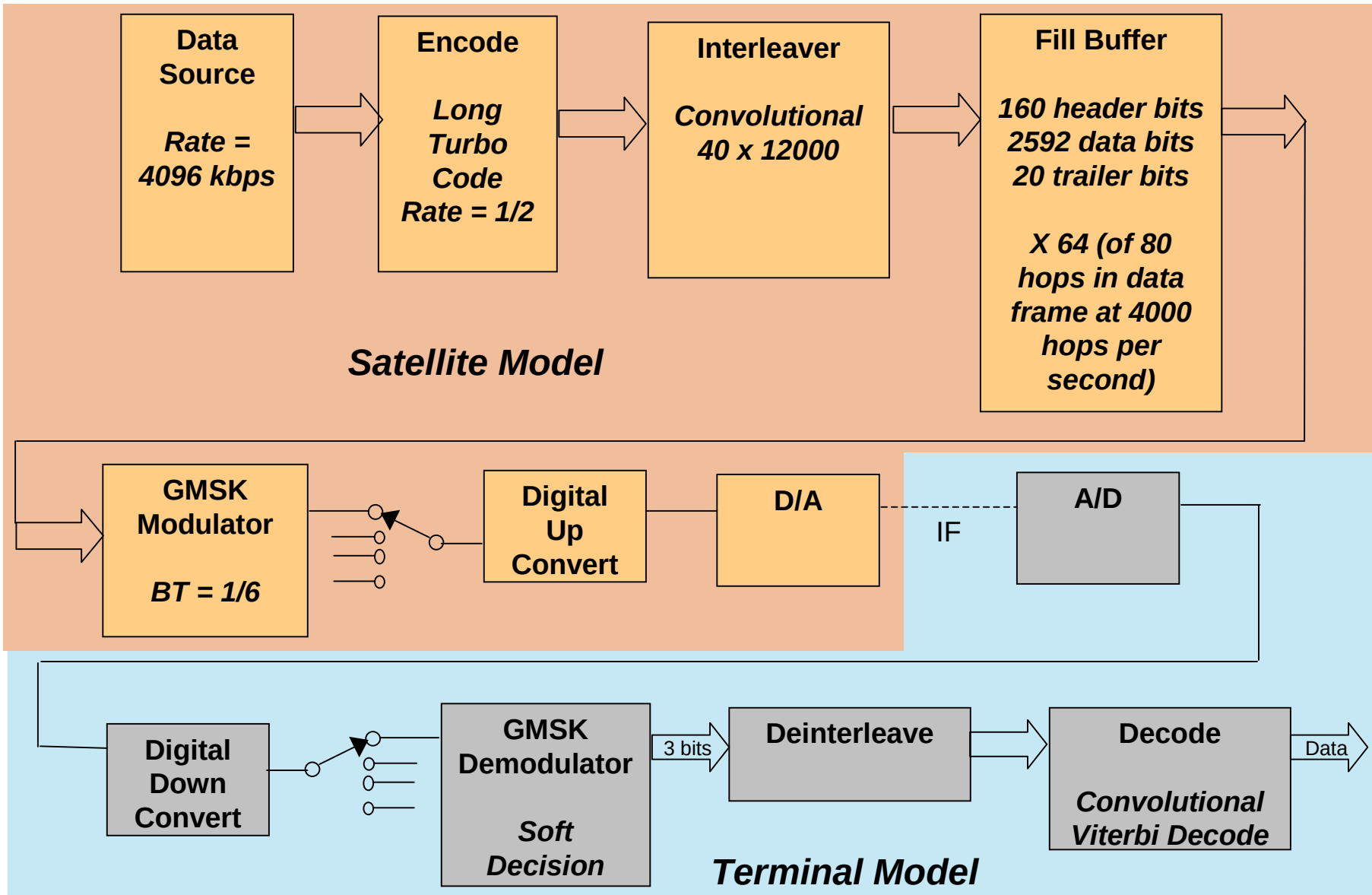
- Experimental waveform is meant to represent the general functionality of modern high bandwidth military waveforms
  - GMSK modulation
  - Turbo encoding
  - Interleaving
  - Hop structuring
- Waveform will be run at a simulated hop rate of 4000 hops per second at an end user data rate of 4.096 Mbps
- Waveform can be conceptualized as a downlink between a processing satellite payload and a receive-only terminal

Experimental Waveform: Link Overview

- Assumes “processing” satellite
- Models satellite modulator and terminal demodulator
- Receive-only terminal functionality



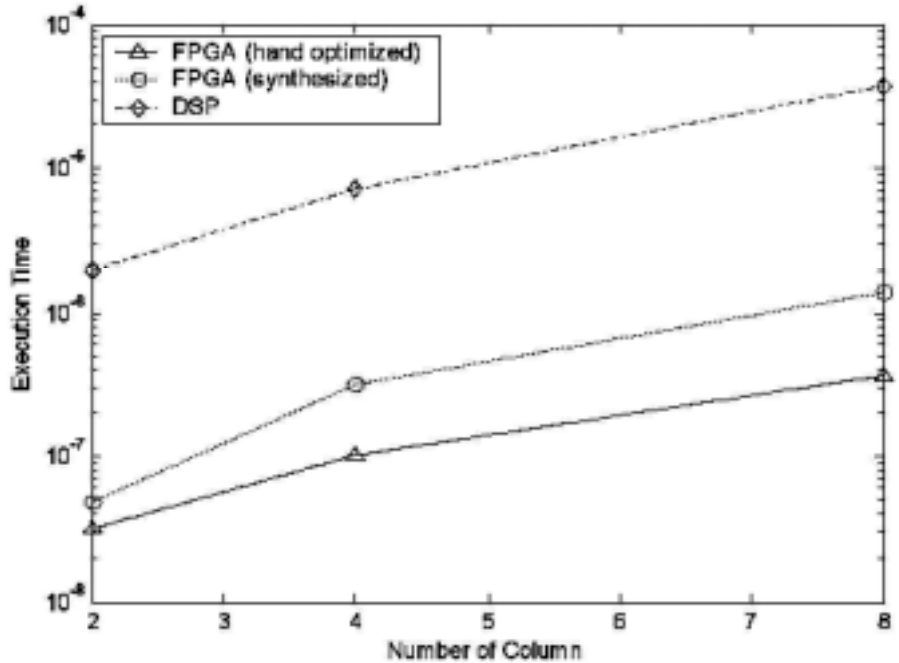
Experimental Waveform



Complexity Trends for Future Waveforms

- Future Waveforms will require increased processing power because of:
  - Increased throughput
    - Factor of 2 to 50
  - More complex processing
    - Bandwidth efficient modulation
    - Other signal processing
      - Turbo coding
      - Multiple Access
      - Frequency Reuse
      - Space Time Coding

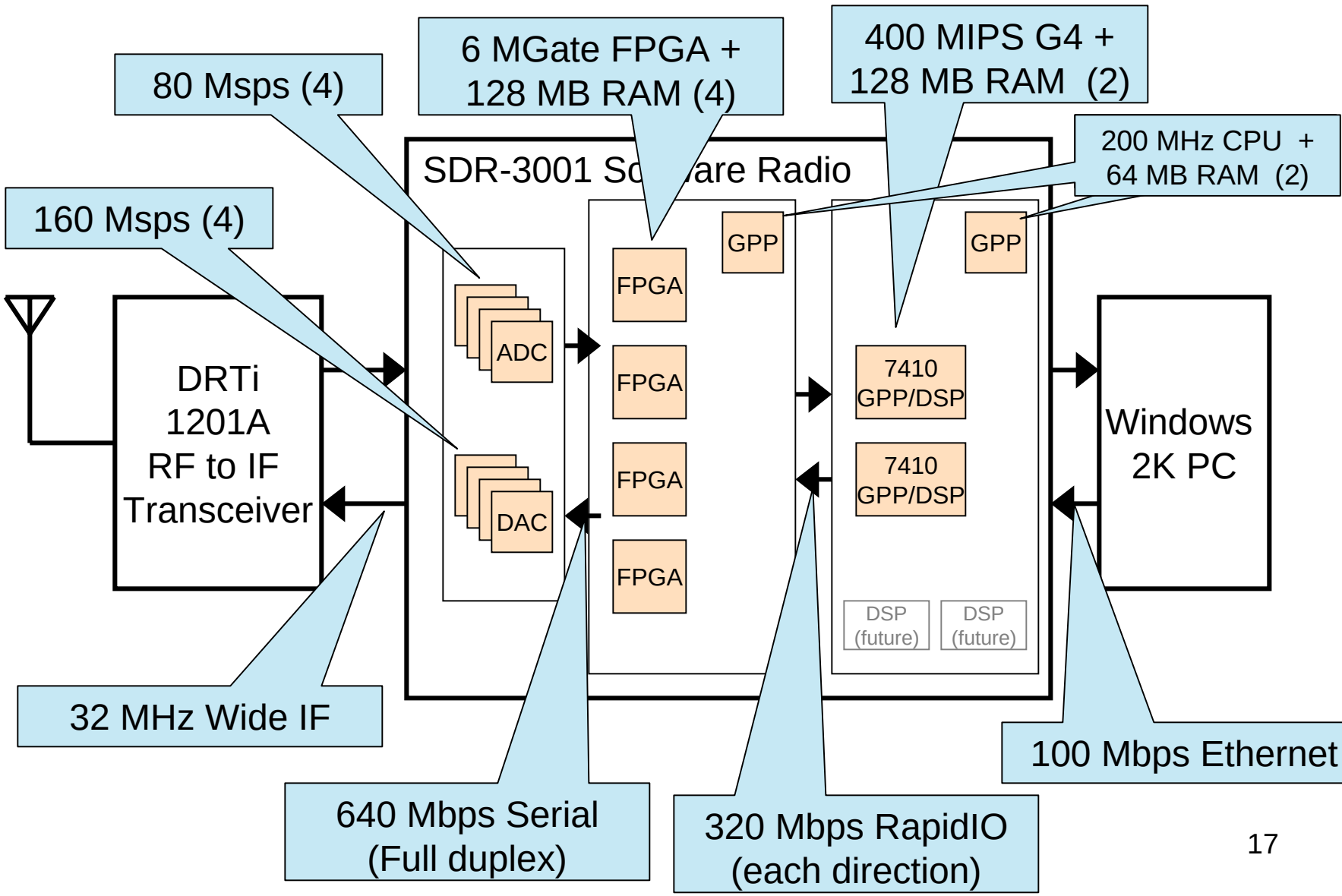
FPGA vs. DSP Performance



Matrix Multiply FPGA vs. DSP

Waveform complexity and required processing power mean that FPGAs and ASICs will be needed for the foreseeable future

Laboratory Configuration



MITRE SCA Lab

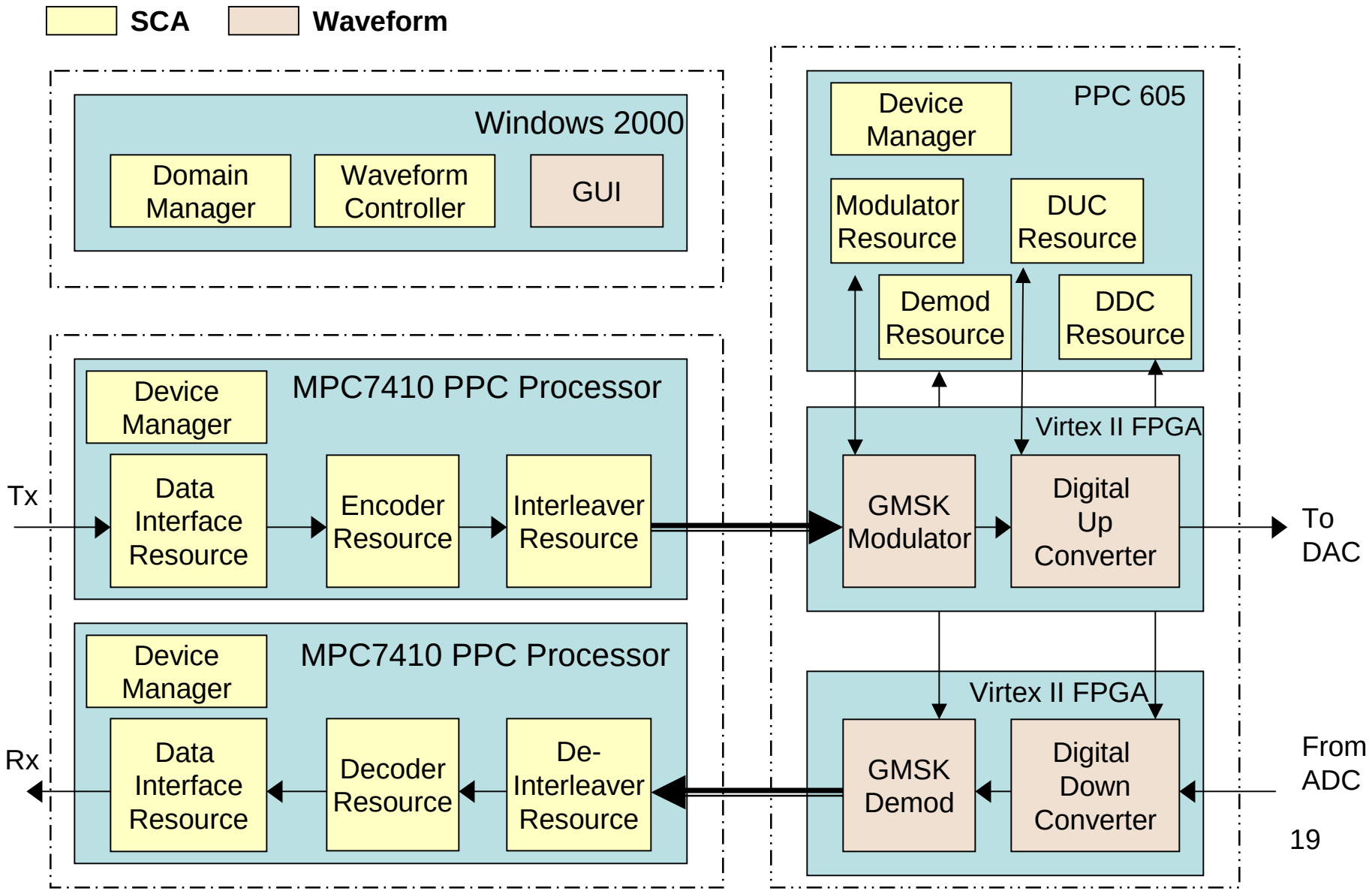
Hardware

- Spectrum SDR-3001 Platform
  - PowerPC MPC7410 ‘G4’ Altivec Processors (2)
    - 400 MHz each
  - PowerPC IBM405GP – embedded controllers (2)
    - 200 MHz, 64 MB RAM, Flash, Ethernet, GPIO, UART, etc
  - Xilinx VirtexII 6000 FPGAs (4)
    - 33,762 slices - ~ 6 Million Gates each
  - 80 Msps ADCs (4)
    - 14 bits each
  - 160 Msps Interpolating DACs (4)
    - 14 bits each
  - 320 Mbps RapidIO
- DRTi 1201A IF to RF Transceiver
  - 20 MHz to 3.0 GHz Tx/Rx Frequency
  - 5 MHz course tuning
  - < 100 µSec tuning speed

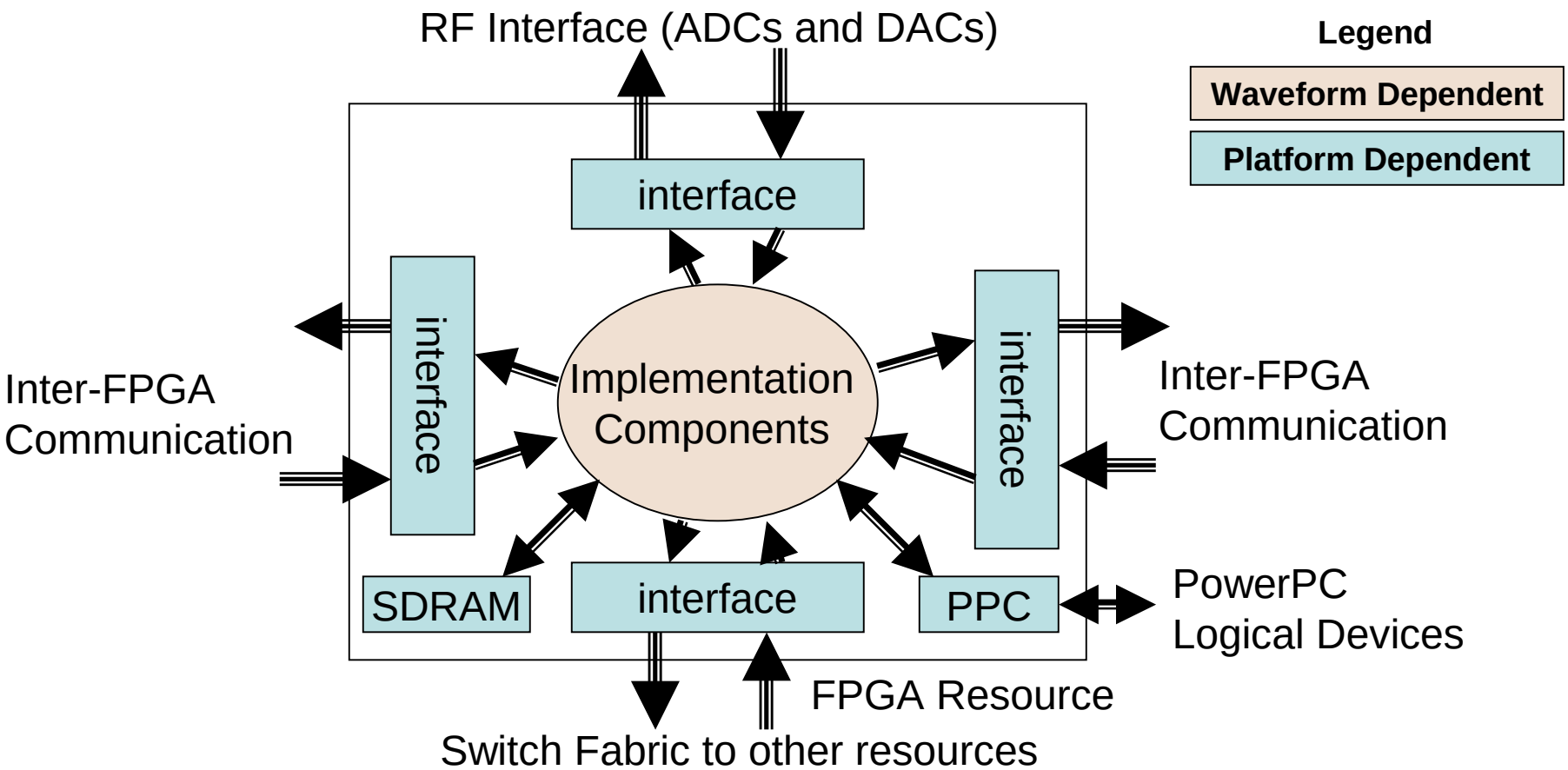
Software

- SCA Core Framework v2.2 (from Spectrum Signal Processing)
- SCA 3.0 HAL-C (developed)
- ACE/TAO ORB
- VxWorks RTOS
- Board Support Package
  - Includes logical devices and device managers for all processing elements of the SDR-3000 system
    - Virtex-II FPGAs
    - PowerPC 7410s
    - PowerPC 450GPs
  - Includes high speed communications capabilities
    - RapidIO switch fabric (*quic*Comm) APIs for inter-board communication
    - Solano for intra-board communication

Mapping Function to Resources

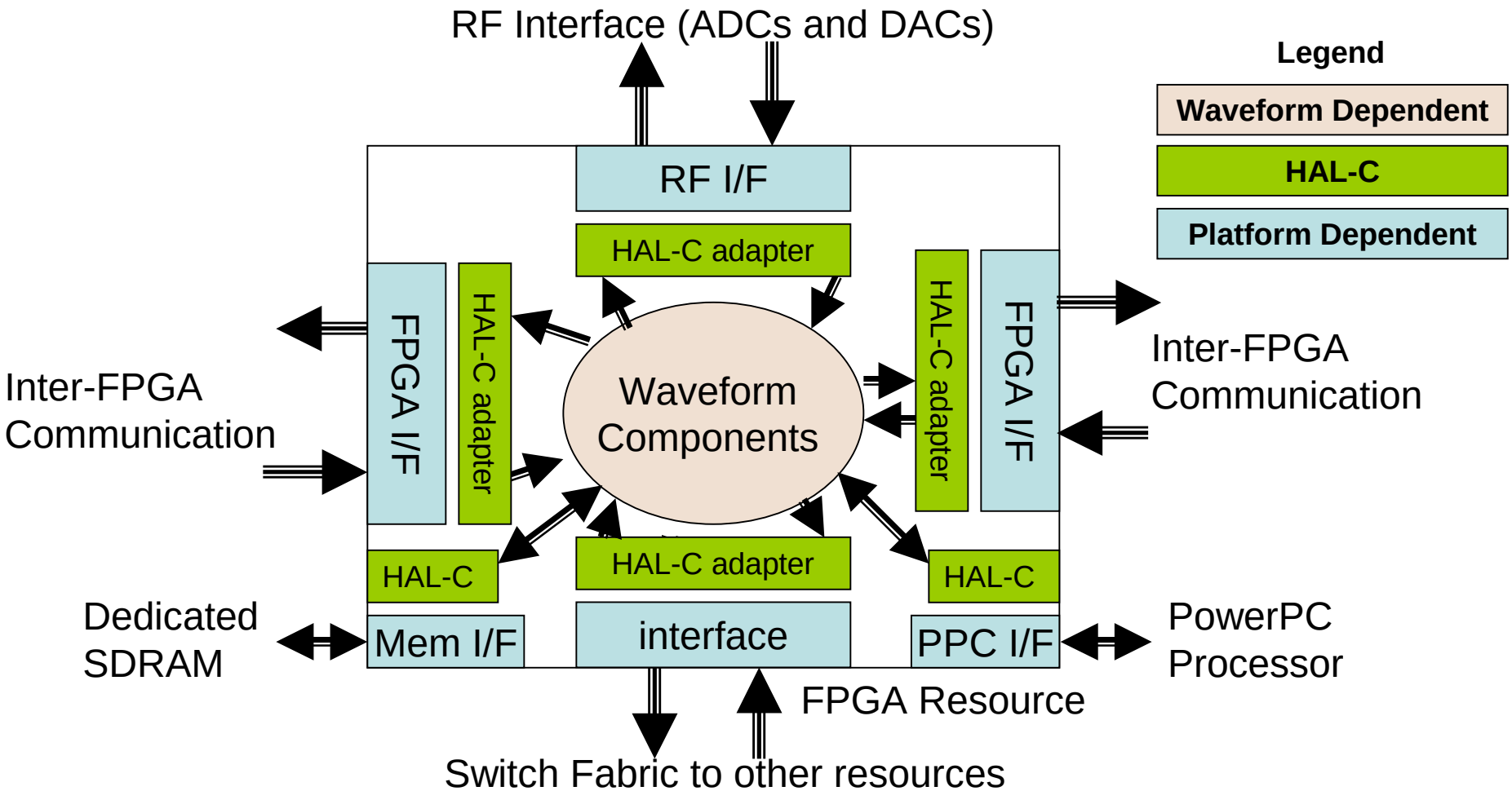


Hardware Isolation – Step 1



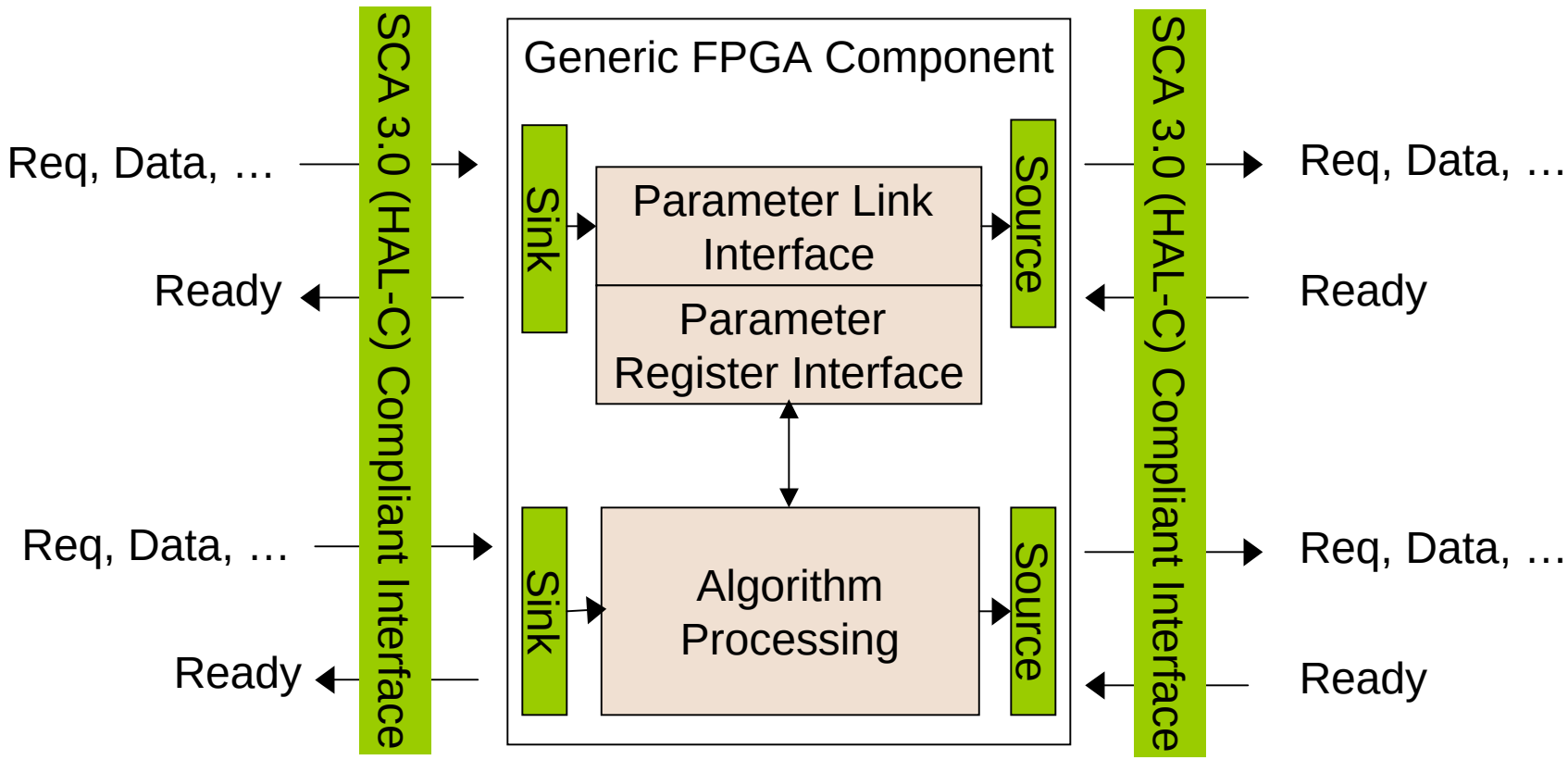
Step 1: Isolate hardware from software (i.e., hardware interfaces are not embedded in waveform dependent code blocks)

Hardware Isolation – Step 2



Step 2: Add HAL-C interconnect technology. As necessary, create adapters for interfacing with off-the-shelf interface components

FPGA Component Interfaces



- HAL-C provides a defined standard
- HAL-C must be capable of handling high data rates and provide low latency for timing sensitive applications

Non Real Time Setup and Control

HAL-C

Status of Activities

- Experimental waveform implementation will be completed by December 2004
  - Includes implementation of HAL-C
  - Includes waveform definition (SCA domain profile)
- Experiment/test definition in progress
  - Performance tests
    - Timing predictability
    - Latency
    - CPU and memory utilization
  - Porting tests
    - FPGA to DSP
    - GPP to DSP

Observations

- Hardware Abstraction Layer – Connectivity (HAL-C)
  - To achieve portability goals the interface definition must become a defined standard
  - To be useful for wideband MILSATCOM waveforms, HAL-C must:
    - Be capable of handling high data rate requirements and provide low latency
    - Be flexible and efficient to implement
  - Providing an abstraction layer for Specialized Hardware will permit hardware to be selected based on price and performance without the need to redevelop algorithm software
- For FPGA “code,” need to develop an abstracted interface that does not use FPGA absolute addresses
  - As FPGA code is compiled, different physical addresses are assigned by the compilers for control, status bits, and registers within the target hardware
  - Need to be able to use function and variable names if the waveform developer is to be abstracted from the absolute hardware addresses
- SCA 3.0 fails to address Quality of Service (QoS)
  - Needed to support dynamic reconfiguration

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Industry is converging on SCA solution for above 2 GHz MILSATCOM Terminals