



Experimentation of MARTE in the Industry **An early adopter case study**

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MARTE fosters model-based design of real-time and embedded systems in Thales

- ▶ Why we need a UML profile for Real-Time and Embedded
- ▶ Involvement of Thales in the definition of MARTE
- ▶ Case study: a generic Flight Management System
- ▶ Applying MARTE to design a generic FMS



THALES

UML is emerging as a possible solution to address the Real-Time and Embedded domain

- ▶ A large audience in the Software Engineering community
- ▶ Extension capabilities through UML profiles (e.g. SysML)
- ▶ But lacks key notions to fully address RTE specifics (time, resource, scheduling)

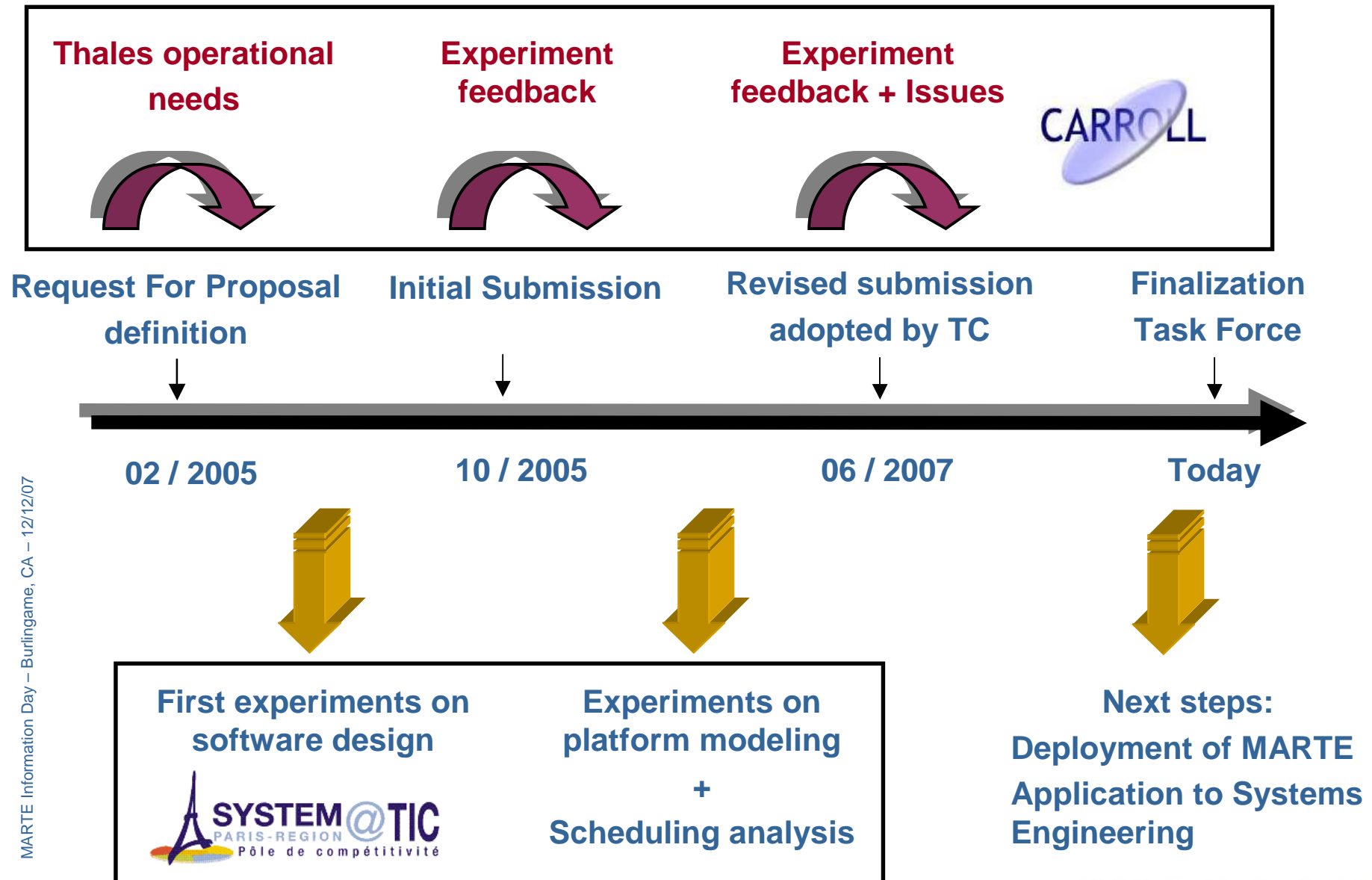


Previous attempts to adapt UML to the RTE domain

- ▶ Academic initiatives
- ▶ Commercial tools: ARTiSAN, Rational Rose RT, Rhapsody (Real-Time UML)
- ▶ UML profile for Scheduling, Performance and Time (SPT)
 - ▶ The first OMG adopted specification in this domain
 - ▶ Defines annotation mechanisms to perform quantitative analysis
 - ▶ Required major improvements over time

Extensions to UML 2 are required to deal with modeling and analysis of Real-Time and Embedded systems

Involvement of Thales in MARTE

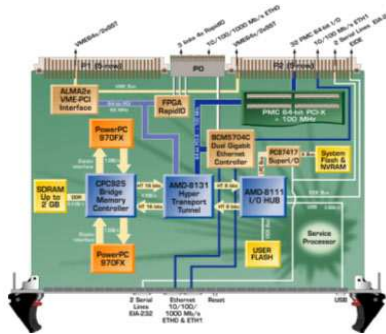


A software-intensive avionics system

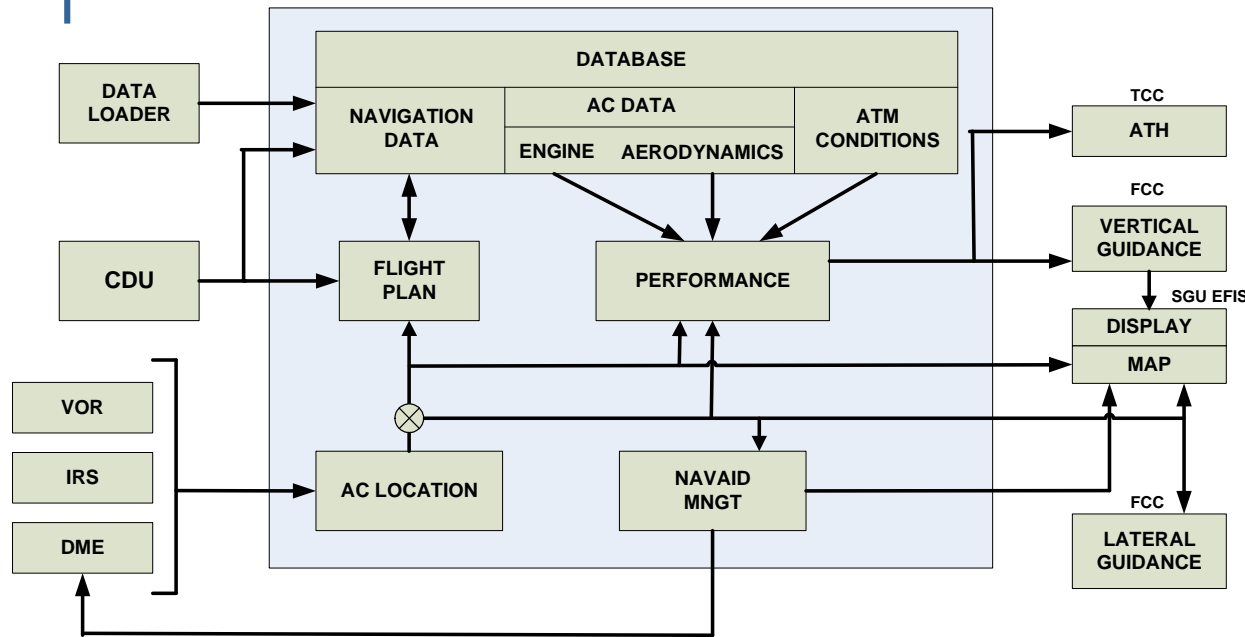
- ▶ Automated navigation (guidance for related devices: AP / FD / ATH)
- ▶ Lateral and vertical trajectory optimizations
- ▶ Fuel consumption and forecast
- ▶ Flight data display

A safety-critical, hard-real time, embedded system

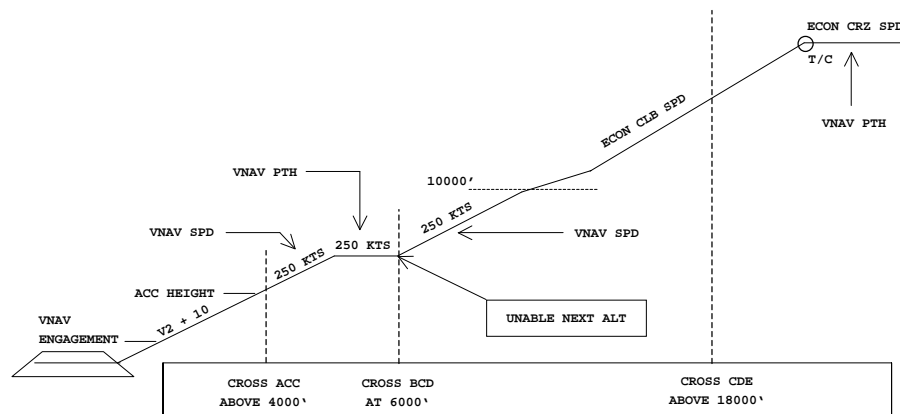
- ▶ Strict latency on processings and communications
- ▶ Strict jitter constraints
- ▶ Dimensioning of buses, FIFOs and CPU power



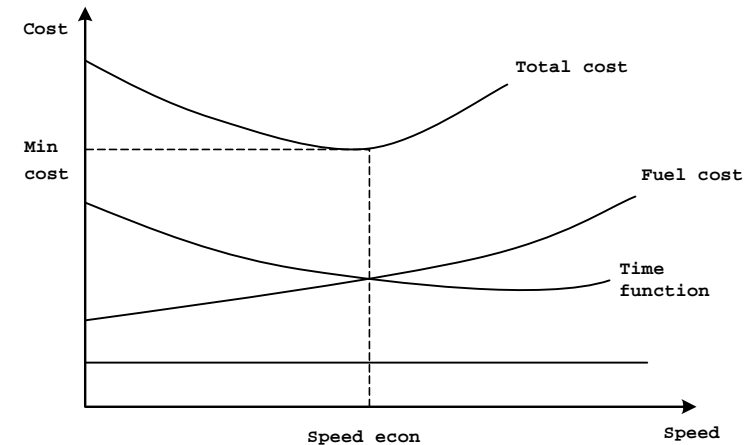
The case study: a generic FMS (2)



FMS block diagram



Lateral and vertical navigation



Fuel consumption / cost index

Early experiments of MARTE required to develop our own tooling

- ▶ MARTE profile implemented in various UML tools (Rhapsody, IBM RSA, MagicDraw)
- ▶ Value Specification Language (VSL) editor consolidated from Papyrus
- ▶ RapidRMA gateway developed for model-based scheduling analysis



Tools integrated through Eclipse / EMF / UML2

Implementation of MARTE for RSA available in open source (EPL)

- ▶ OMG MARTE web site: <http://www.omgmarTE.org>

➔ **System context definition**

- ▶ Use case overview
- ▶ Time constraints on performance scenarios
- ▶ Types and units

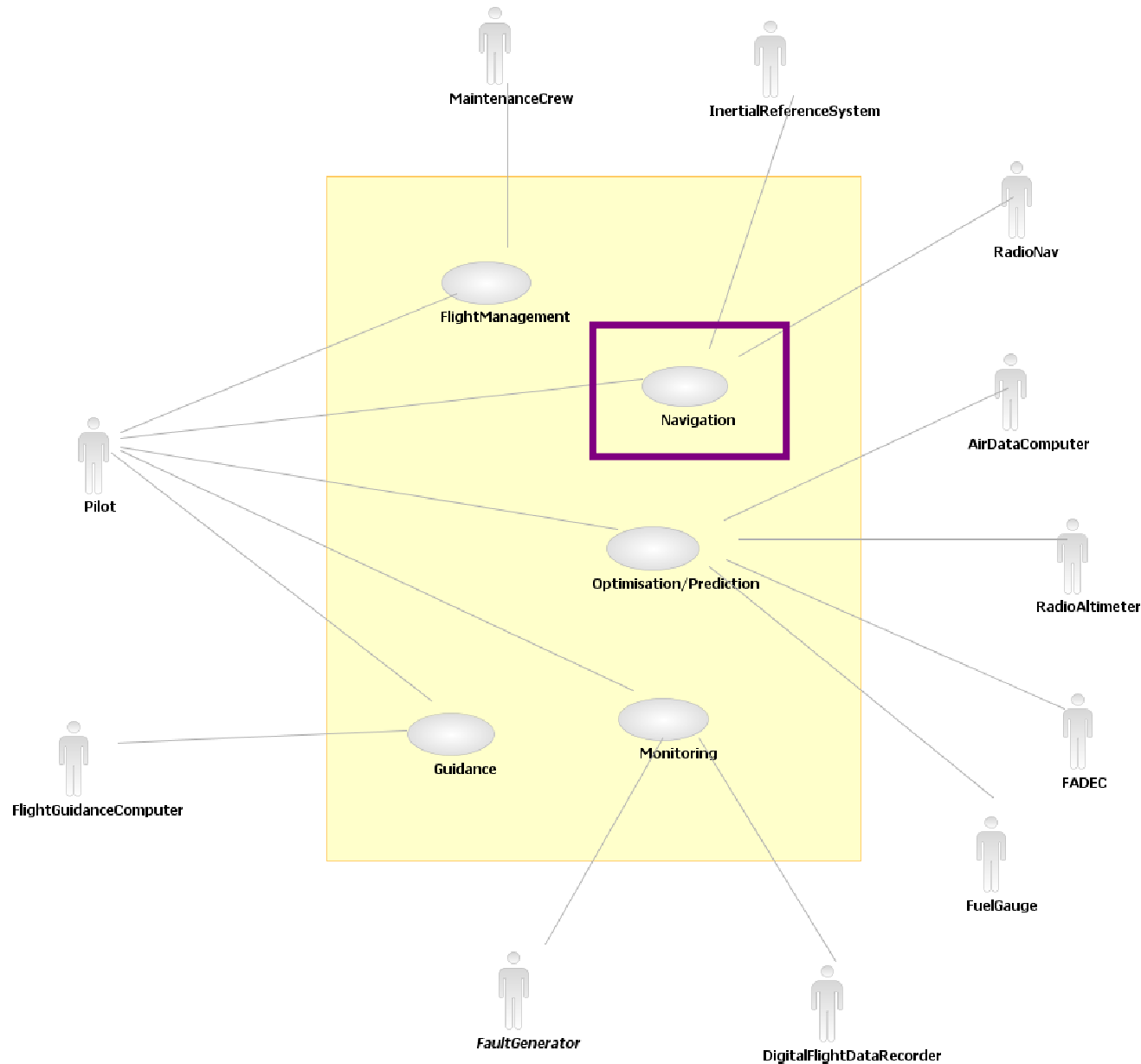
System design

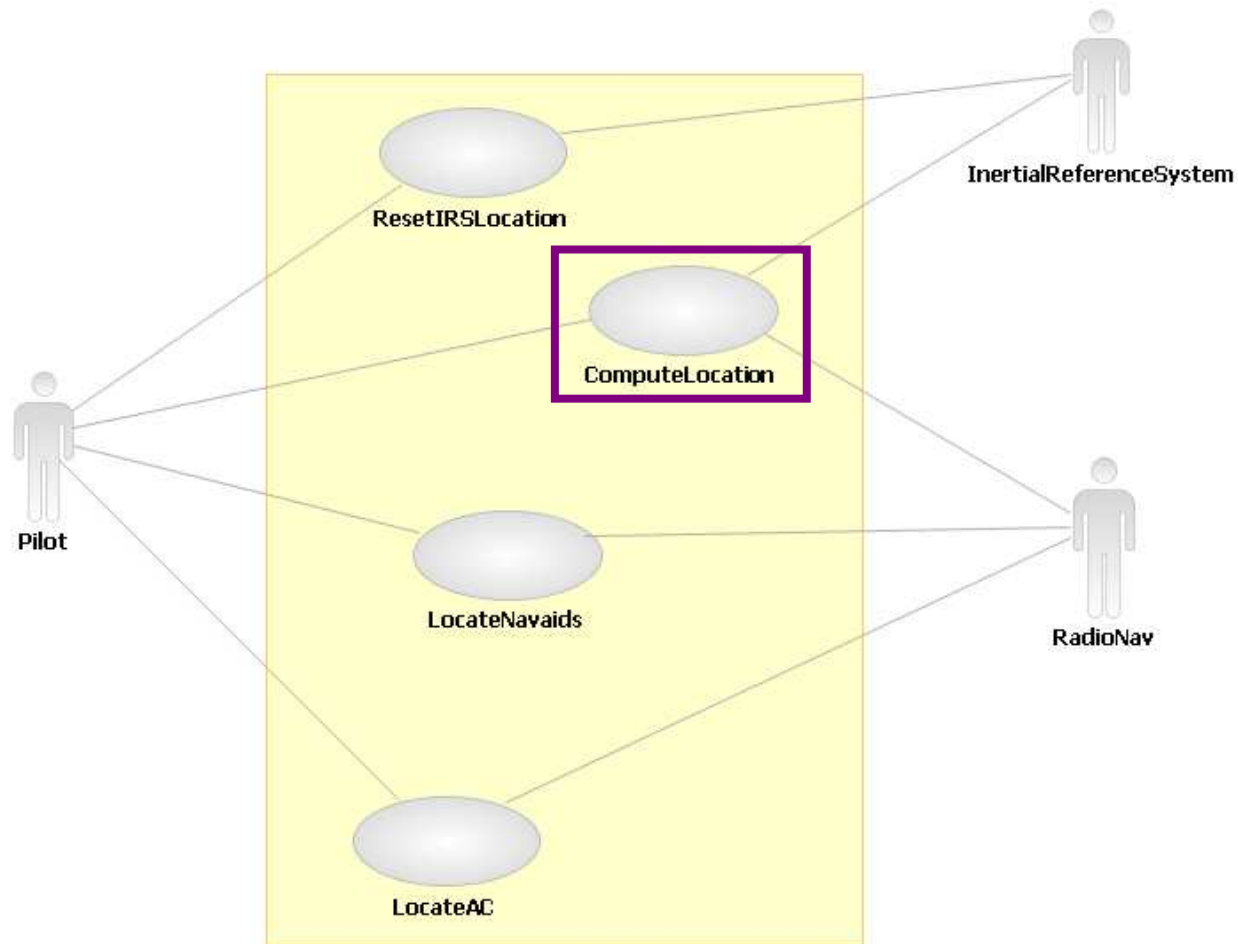
- ▶ Logical decomposition (structure, behavior)
- ▶ Physical decomposition (resources)
- ▶ Allocation

Scheduling analysis

- ▶ Building scheduling analysis model
- ▶ Validate system scheduling with RapidRMA

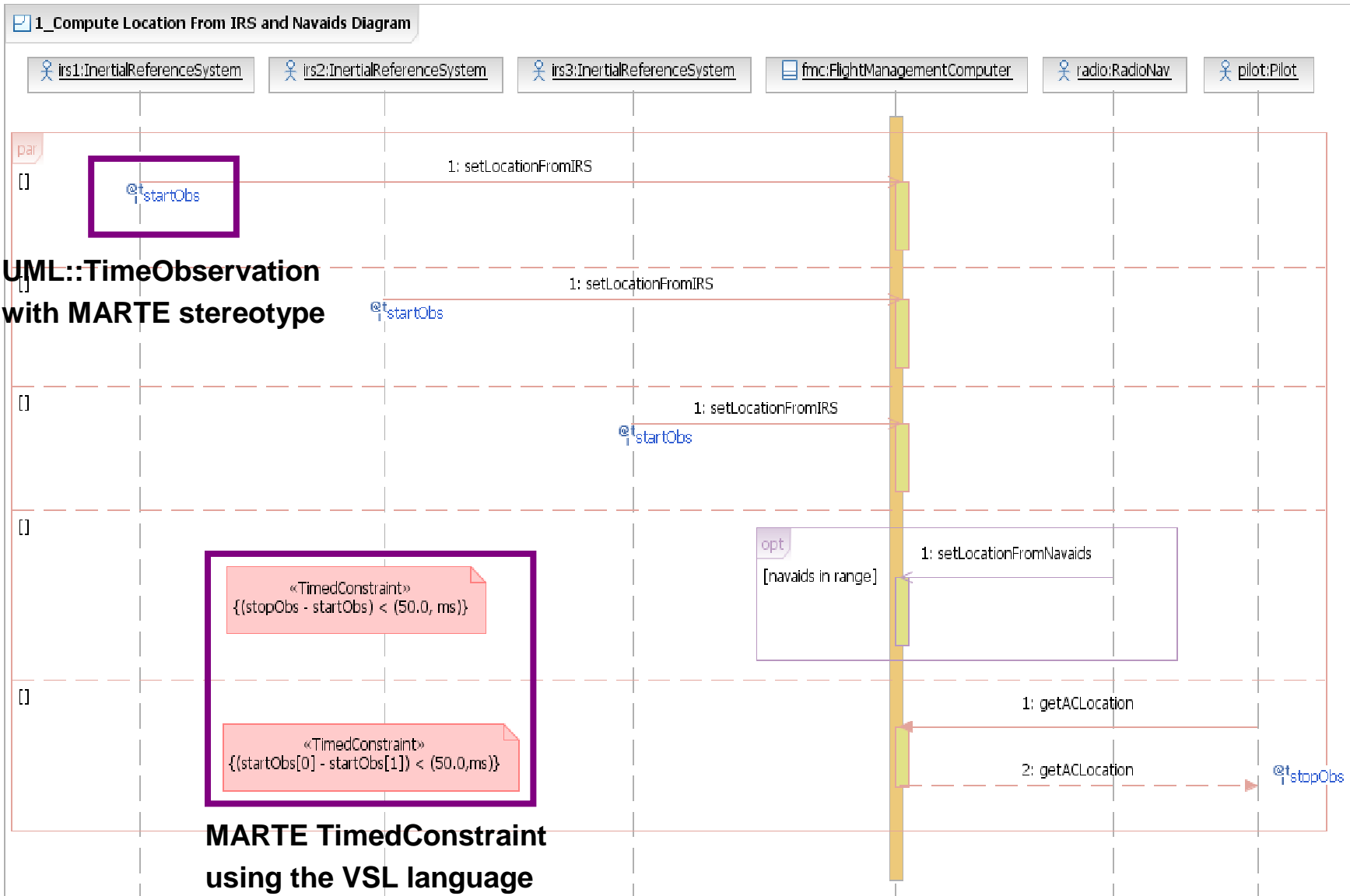
Context and use cases

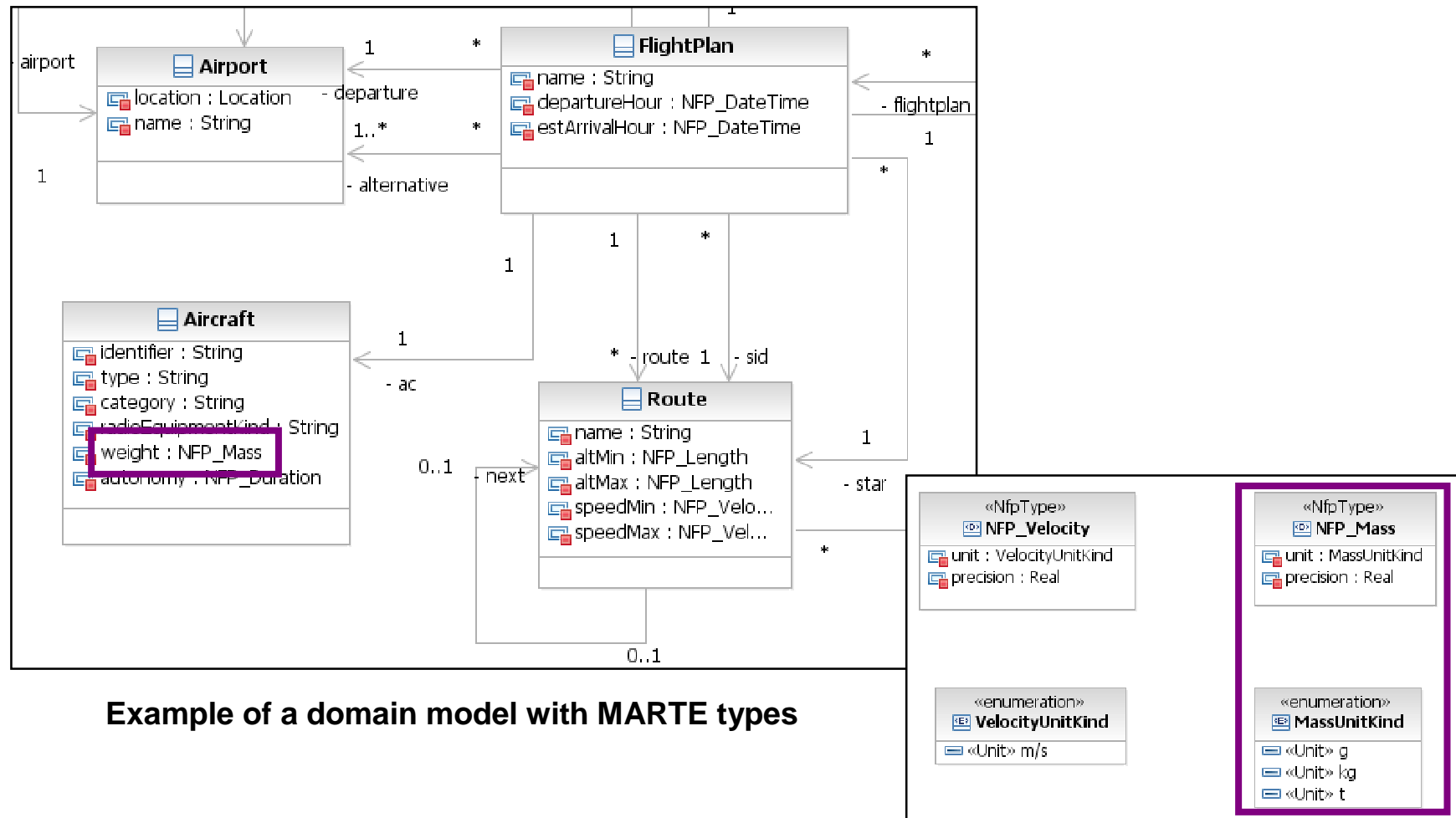




Navigation use cases

Time constraints on performance scenarios

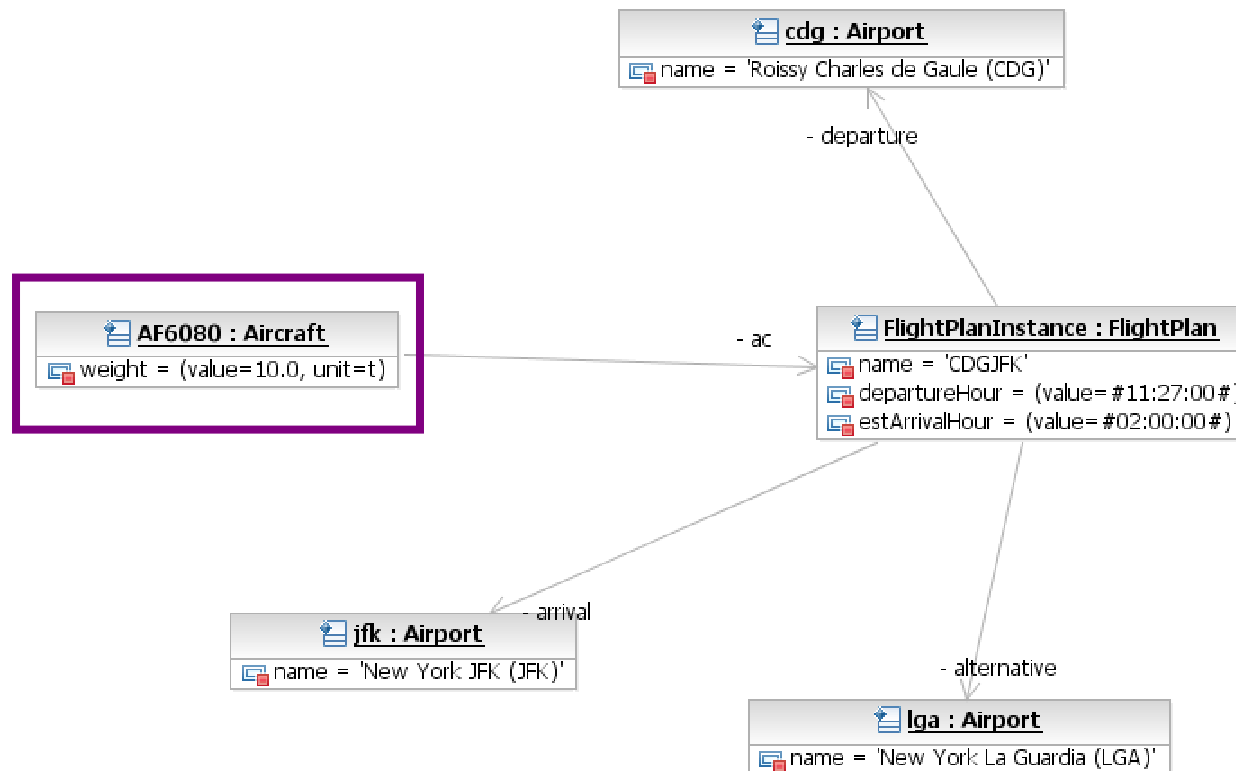




Example of a domain model with MARTE types

User-defined types and units that extend the MARTE Library

Using types and units in VSL expressions



Units and types used along with value specifications

System context definition

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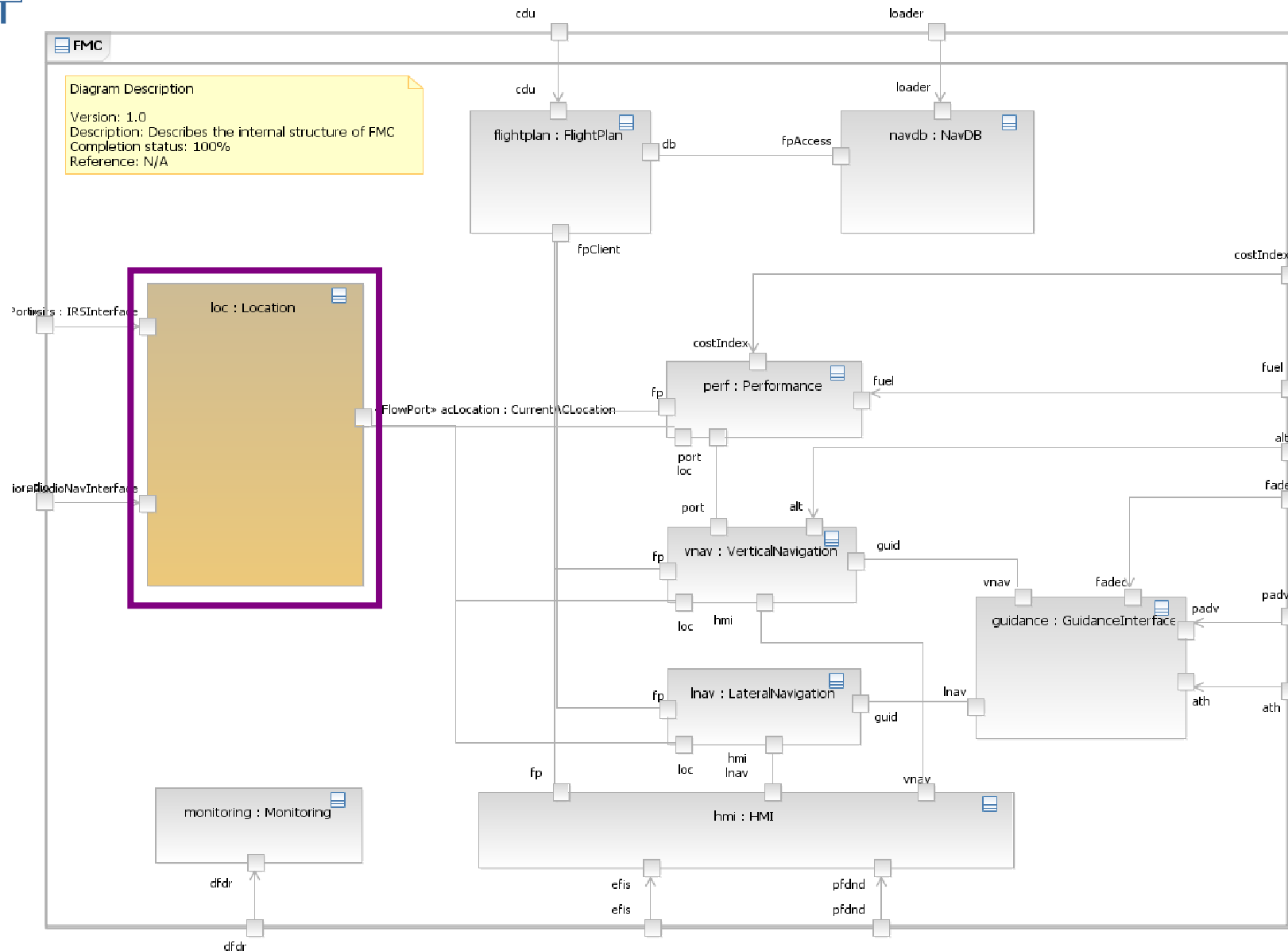
➔ System design

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Logical decomposition (structure)



Logical decomposition (structure)



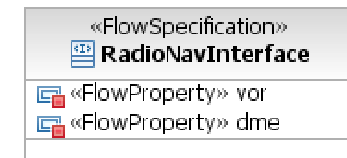
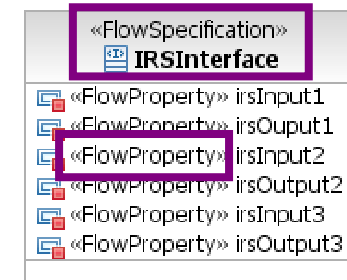
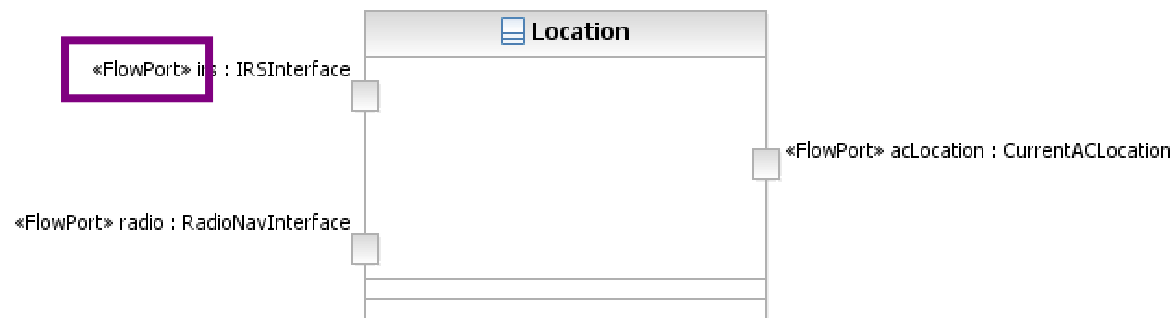
Diagram Description

Version: 1.0

Description: Describes the interfaces of the location component

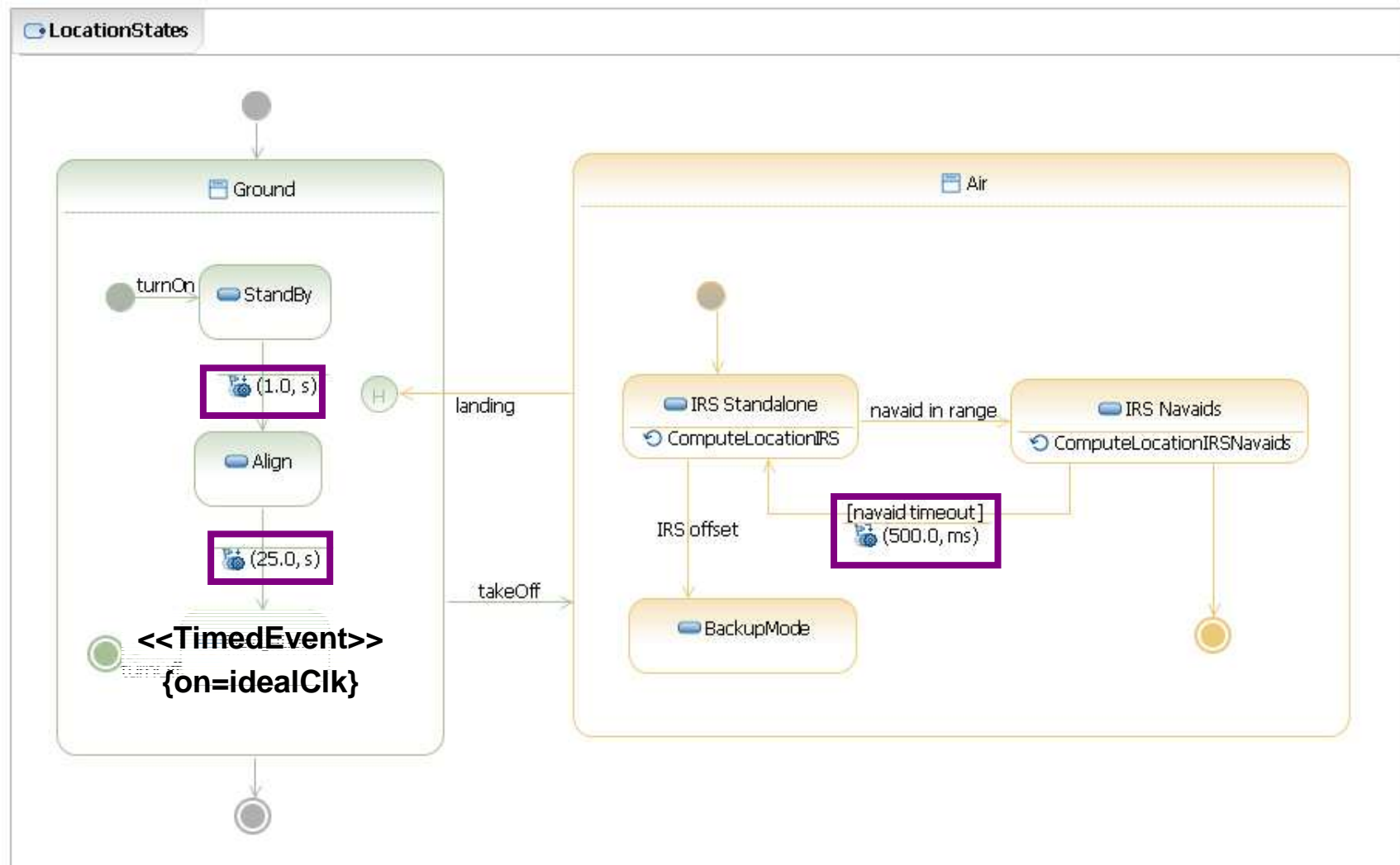
Completion status: 100%

Reference: N/A



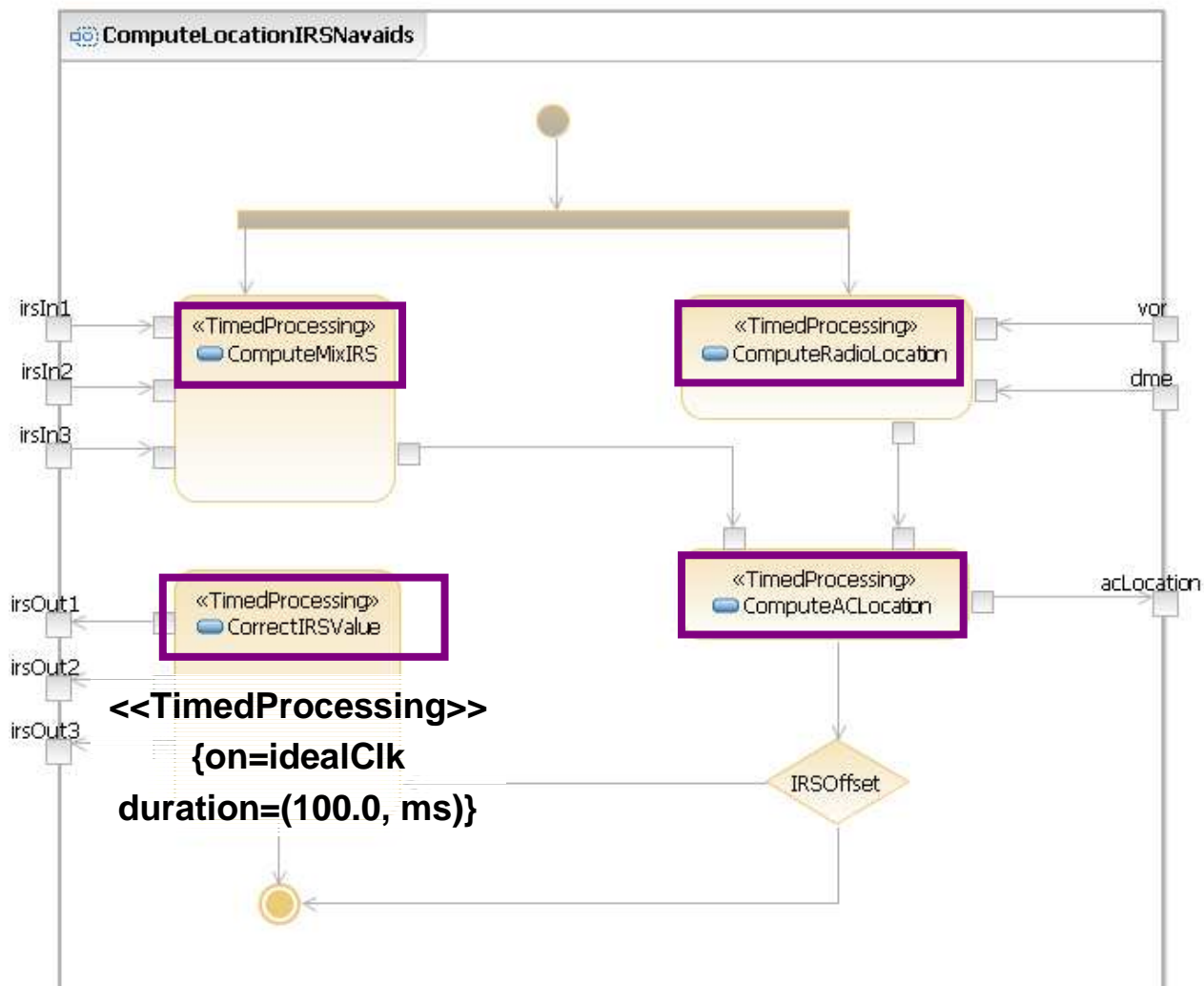
Flow-related concepts inspired from SysML

Logical decomposition (behavior)



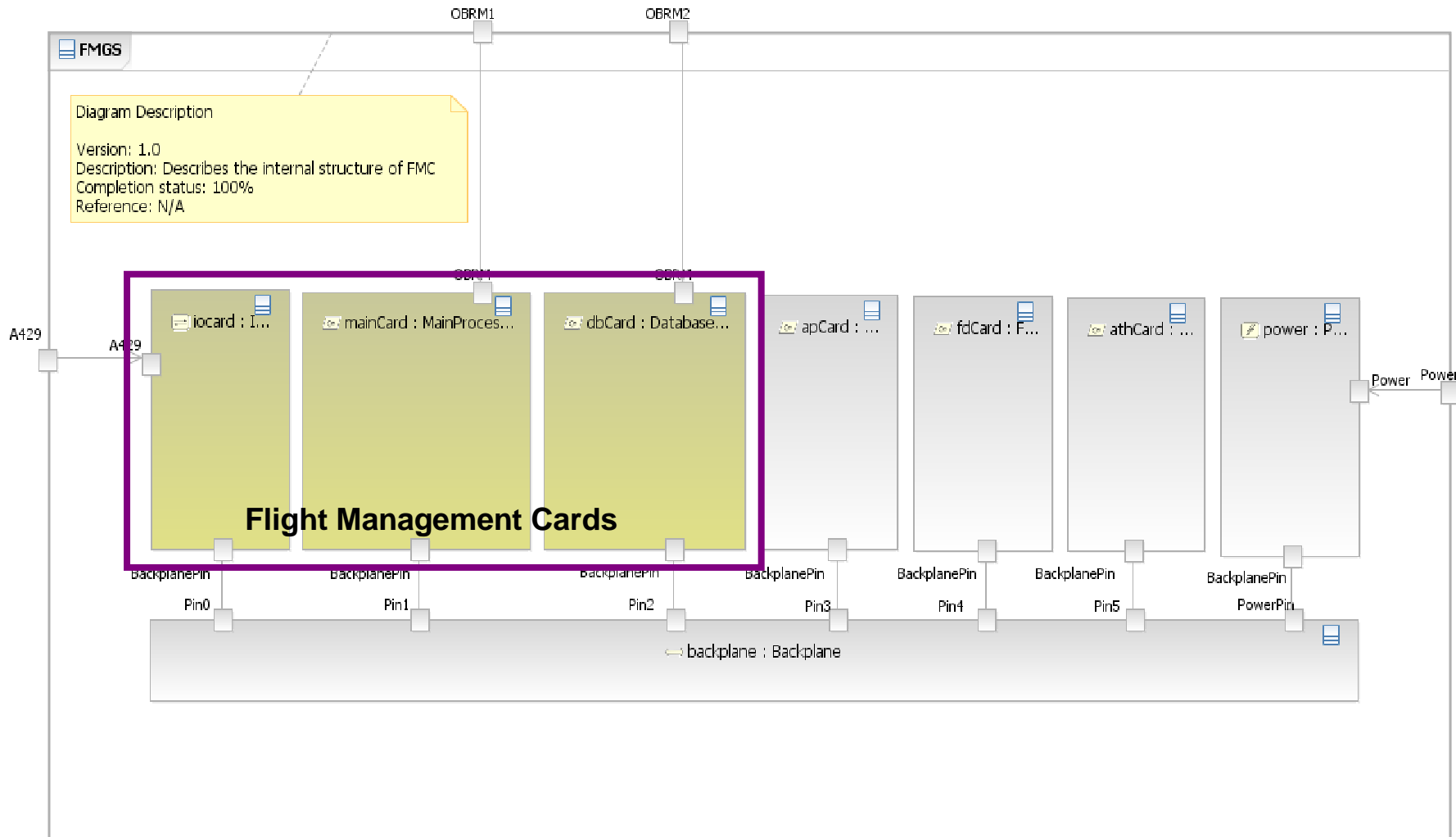
Time-triggered transitions (relies on physical time in this example)

Logical decomposition (behavior)



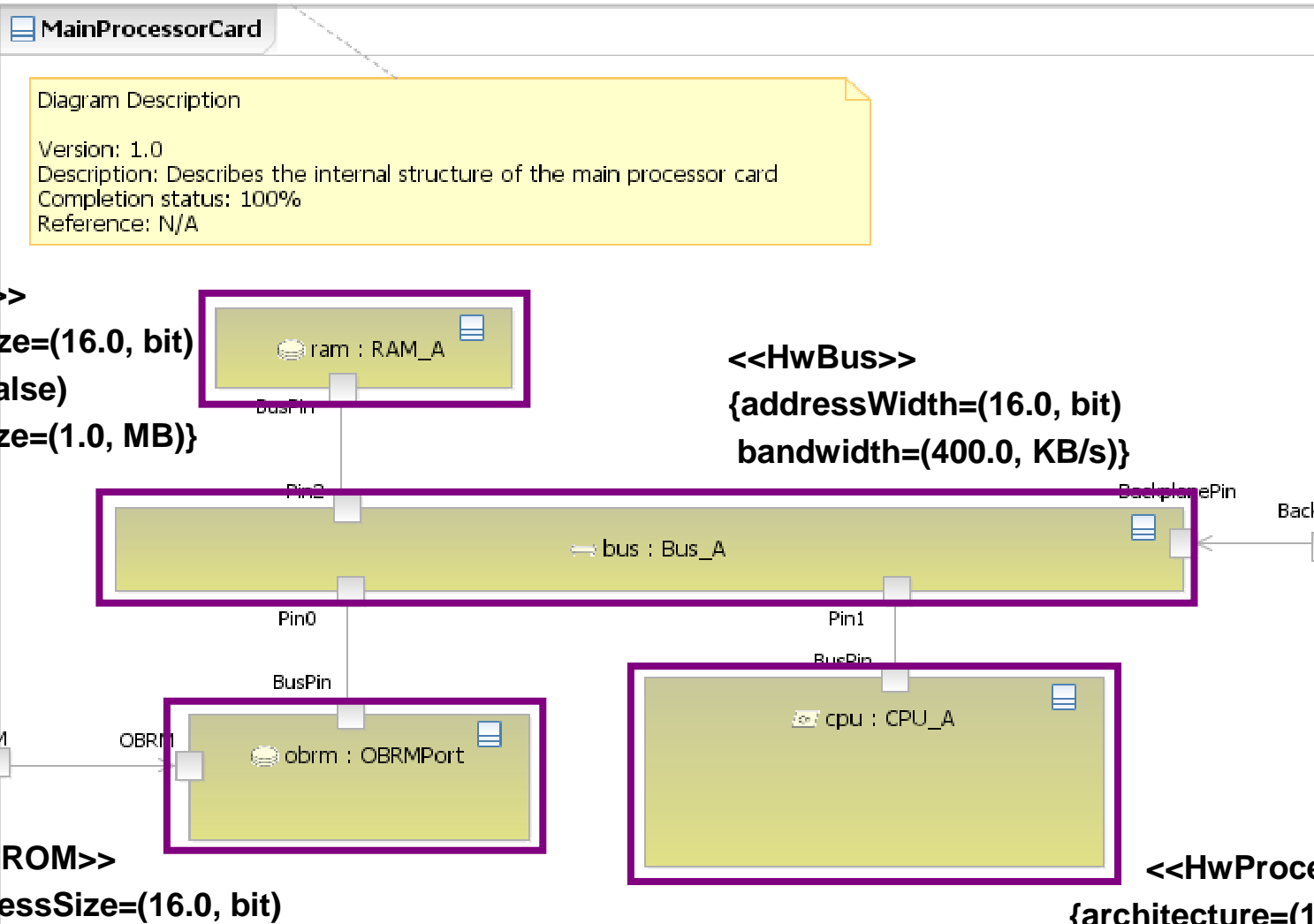
Timed processings (with a duration) in an activity diagram

Physical decomposition (hardware)

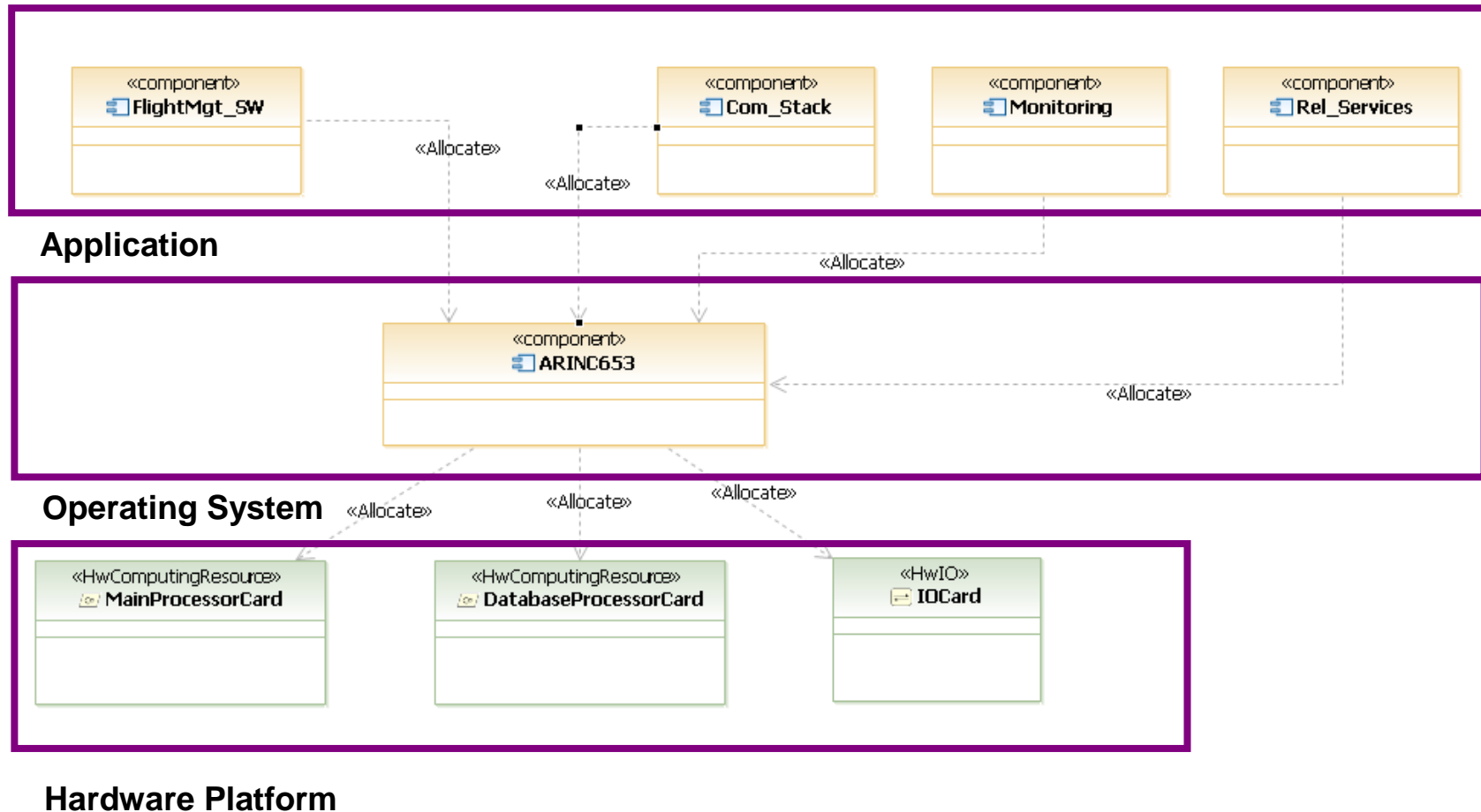


Top-level decomposition of the Flight Management and Guidance Computer

Physical decomposition (hardware)



Physical decomposition (software artifacts)



System context definition

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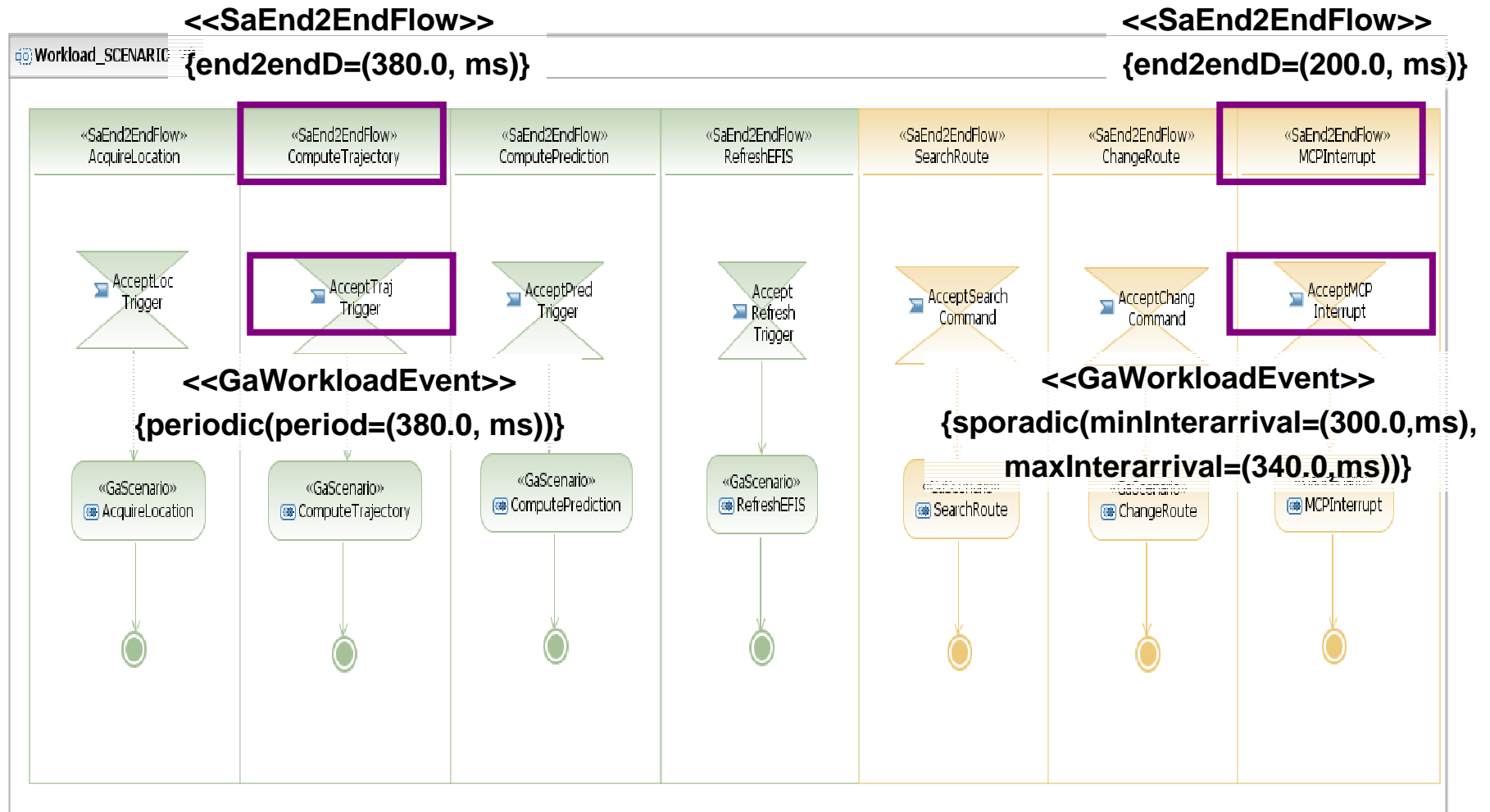
System design

- ▶ Logical decomposition (structure, behavior)
- ▶ Physical decomposition (resources)
- ▶ Allocation

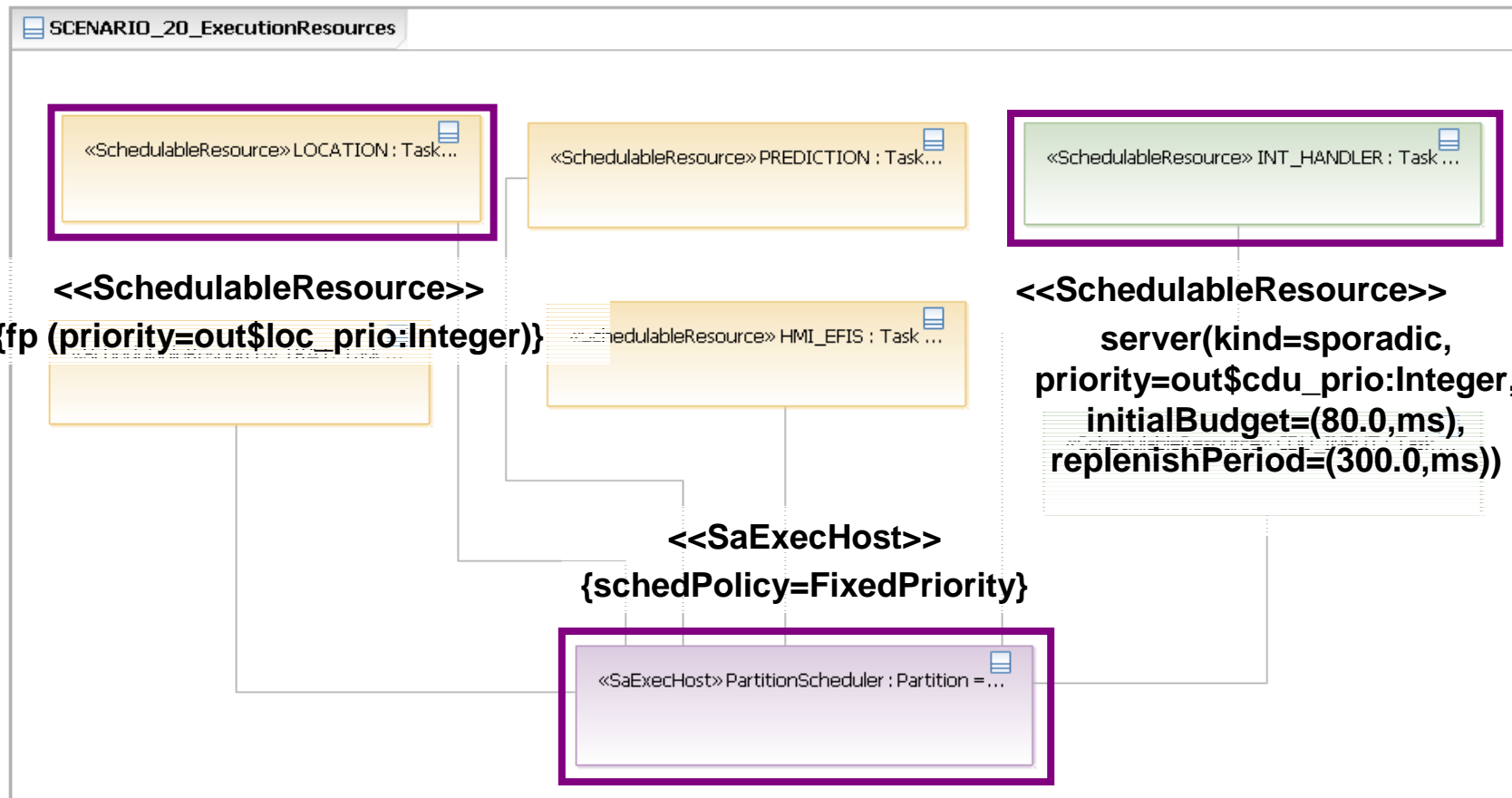
➔ Scheduling analysis

- ▶ Building scheduling analysis model
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Scheduling analysis (workload)



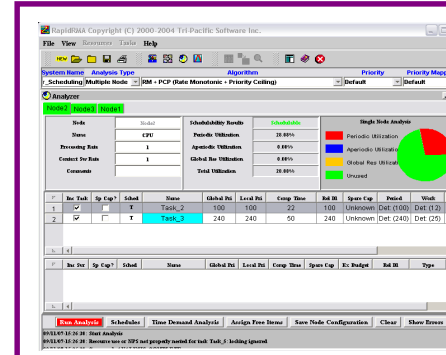
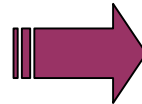
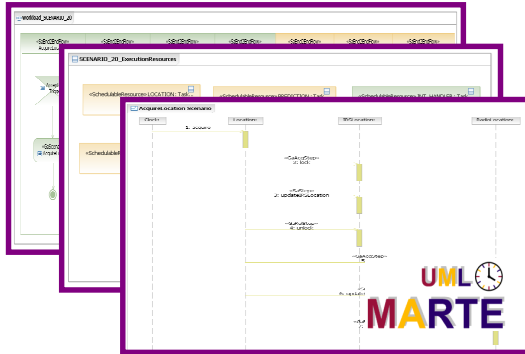
Scheduling analysis (resource)



Scheduling analysis (scenario)

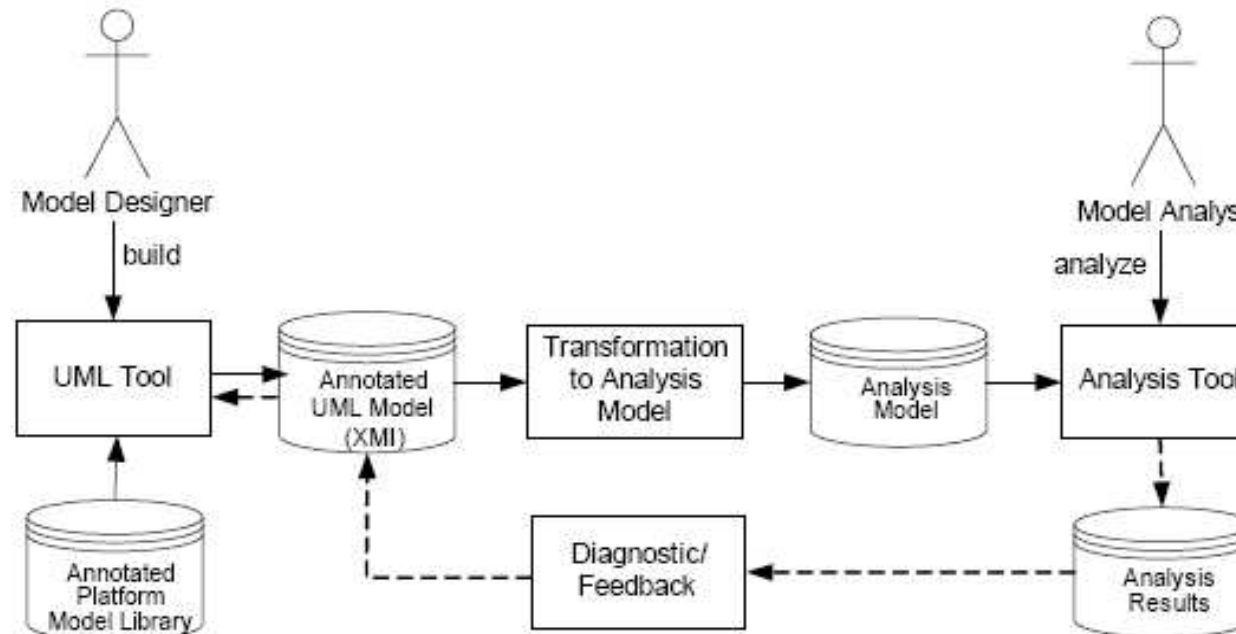


MARTE to TriPacific RapidRMA



Compute a schedule for tasks in a partition

Help dimensioning the sporadic servers



MARTE has provided the necessary support for modeling and analyzing our system

- ▶ Modeling Time and NFPs
- ▶ SW / HW platform design
- ▶ RMA scheduling analysis

UML and MARTE are key enablers for model-based analysis and early validation

We are eager to see tool vendor implementations of MARTE

