PRESTO: Improvements of Industrial Real-time Embedded Systems Design and Development

Imran Quadri, PhD.

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Overview

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Introduction
Context: Real-Time Embedded Systems
Current design challenges

• Real-Time Embedded Systems (RTES) are exponentially increasing in complexity

• The “Design Productivity Gap” between Hardware and Software development
  - Increase in Time to Market and Overall Costs
What to do?

• Effective design methodologies needed
  o Elevation of design abstraction levels
    • Hand tuned coding at Register Transfer Level (RTL) ➔ High Level Synthesis (HLS) ➔ . . . .
  o Co-Design (Y-Chart)
  o Component based approach (e.g. AADL)
  o IP-Reuse (e.g. OPC; IP-XACT)
  o Model Driven Engineering

• Increasing synergy
• Separation of concerns
PRESTO
(ImProvements of industrial Real Time Embedded SysTems deveOpment process)
PRESTO Overview: Objectives

• Improve upon current RTES practices
• System Level Exploration
  o To enable early functional and performance analysis, platform optimization and validation
  o Test traces exploitation (e.g. System functional/non functional requirements)
PRESTO Overview: Consortium Information

- Coordinator: Teletel (Greece)
- Budget: 8.6 M€
- Total Effort: 852 pm
- Start date: April 2011
- Duration: 36 Months

- 5 countries
  - 13 partners (8 SMEs)
PRESTO Overview: Consortium Information

Finland
- VTT
- MetaCase
- SarokalSolutions

Italy
- THALES

Greece
- teletel
- MILTECH
PRESTO Overview: Design Methodology

- Application models / Workloads
- Execution platform models
- Allocation / Mapping
- Simulation
- Execution Platform

Design Flow → Feedback
Modeling RTES for System Level Exploration

- System modeling (Hardware/Software and their allocation)
  - Approach: Classical Y-chart
  - Standards/Specifications:
    - MARTE, EAST-ADL, SDL, SCA ...
  - Integrating aspects:
    - Timing,
    - Performance,
      - WCET analysis
    - Schedulability
- Model refinements
  - Trace integration and visualization at model level
Trace Driven Analysis

• **Common Test Trace** format definition, generation and exploitation

• Types of traces:
  o Test cases/Specification traces,
  o Raw/Execution traces
  o Filtered traces/result scenarios

• Trace filtering
  o Relevant traces to reduce set of inputs/states for each trace

• Functional properties verification
  o End user initial system requirements, causal properties, etc.

• Non functional properties verification
  o Deadlines, periodic, sporadic behaviors, etc.
Software Design Flow Improvement

- Temporal logic in test scenarios
  - **Timing constraints**: Rate, latency, jitter, synchronization, etc
- Code instrumentation
  - Automatic code generation
- Trace generation, comparison
- Functional properties verified by generated traces from test executions
- Non functional properties verified by means of performance analysis tools
Hardware/Platform Design Flow Improvement

- Initial evaluation results from high level models via trace results
  - Performance estimation of application execution platform
- Virtual platforms
  - Application software binaries onto platform model (Simulation)
  - Compare different performance simulation models
- Simulation/Execution platform implementation results comparison
  - Useful for fast prototyping tool performance predictions
  - Refining initial platform models
End user case studies (MILTECH)

- Automated Test Equipment (ATE) for on-board communications based on SpaceWire (SpW)
  - Protocol Validation & Testing System for satellite on-board communications
  - SpaceWire standard support
  - Protocol Validation & Testing
    - Test cases development & execution
    - Protocol Emulators
End user case studies (THALES C&S)

- TDMA radio protocol case study
  - Part of a “Time Division Multiple Access” Radio Protocol
  - Supports only a single traffic corresponding to the transmission of short messages with fixed length
  - More details in subsequent demo
End user case studies (continued)

- **THALES Italy**
  - Frequency Hopping Ultra Wide Band (FH UWB) application for indoor position

- **TELETEL**
  - MANET device case study

- Several internal experiments for improving design practices
  - For e.g. VTT’s FFmpeg application implementation on Open Virtual Platform (OVP), **Panda Board**
Challenges in PRESTO

• Interexchange between:
  o Different standards, specifications or languages (**MARTE, SCA, SysML, AADL, EAST-ADL, fUML, SDL, SystemC ...**)
  o Different tools (**Modelio, MetaEdit+, Spectra CX, TimeSquare, ABSOLUT, MOSES, MSC Tracer...**)

• Adapting different end user design flows to the PRESTO methodology

• Positive influence on RTES community
Conclusion
Conclusion

• PRESTO
  o From high level design abstraction levels to execution platform implementation
• Improving existing RTES practices in several application domains
• Contribute to future revisions of OMG standards
  o MARTE, SysML...
• Demo———
Questions ?
Thanks!

Imran Quadri
SOFTEAM | ModelioSoft
Imran.quadri@softeam.fr

PRESTO Project Web Site:
http://www.presto-embedded.eu/

SOFTEAM R&D Web Site:
http://rd.softeam.com

ModelioSoft Web Sites:
http://www.modeliosoft.com
http://www.modelio.org
Modeling solutions.