Software Radio
Cooperative Research Project (SRCRP)

OMG SBC
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Agenda

• Program Overview
• Architecture Overview
• QPSK Porting
• FM3TR Porting
• Summary
Software Radio Cooperative Research Project (SRCRP)

Bi-lateral project sponsored by the JTRS JPEO to promote SDR / SCA concepts Internationally
SRCP Goals

• Promote the Software Communication Architecture (SCA) internationally
• Demonstrate SDR concepts (i.e. common architecture, portability and interoperability)
• Discover what prevents waveform applications from being portable
  – Develop guidelines to avoid portability issues
• Learn what savings in cost and time are possible when using portable waveforms
• Evaluate whether certification improves portability
  – Core Framework Certification
  – Waveform Application Certification
• Create waveform applications that are truly portable
**SDR Architecture**

- SCA 2.2 defines the architecture:
  - Common OS services, Middleware & Radio Framework (CF, Log, etc.)
  - Common Application and Devices interfaces
- SCA does not provide specific Control & Data APIs for Devices and Services
- SRCRP developed Interfaces (Common API) to facilitate WF porting
  - GPP Services (defined in IDL; C++ mapping)
    - I/O and Modem Interface Services (i.e. Serial, Audio and Modem).
  - DSP Services (derived from IDL; C mapping)
    - GPP and RF Interface Services

The key to the porting was the jointly developed “Common API” specification which was realized by both SDRs.
Japan SDR

• Multi-mode Modem
  – 4 independent channels in 19“ rack
  – 4 independent PAs in lower chassis

• COTS with Custom 3u cPCI or 6u module
  – PowerPC750(G3)
  – DSP Sub board on GPP x3
    – TMS320C6415/6416(TI)

• LYNXs OS version 3.1.0a
• CORBA - OSPEE v1.8
• NEC Core Framework
U.S. SDR

- Airborne Multi-Band, Multi-Mission radio
  - Configurable for 1 to 4 channels
  - ARINC-404A \( \frac{3}{4} \) ATR Long form factor
  - COTS with Custom 3u cPCI and 6u modules
    - Pentium (x86)
    - TMS5416 DSP
  - 49 lbs fully loaded w/tray
  - Conduction cooled chassis

- VxWorks OS v5.5.1
- CORBA - ORB Express v2.6.1
- Raytheon Core Framework
Summary of SDR Differences

- Power PC GPP
  - 466 MHz, 16 MB Flash, 256 MB RAM
- Lynx OS (SEGMENTED Memory)
- OSPEE ORB
- TI-6416 DSP
  - 600 MHz, 512KW(16bit) RAM

- Pentium GPP
  - 450 MHz, 96 MB Flash, 64 MB RAM
- Vx Works OS (FLAT Memory)
- Orb Express RT ORB
- TI-5416 DSP
  - 120 MHz, 128KW(16bit) RAM
• Frequency hopping (100 hops per second / hop every 10 ms)
• VHF and UHF military bands (30 MHz- 400 MHz)
• Voice Capability
  – 16Kbps CVSD modulation for voice digitizing
• Specification contains data capability
  – 9600bps rate
  – Reed-Solomon error correction with Interleaving for error spreading
# QPSK SLOC Metrics

<table>
<thead>
<tr>
<th>GPP Components</th>
<th>Pre-Port (V1.3) SLOC</th>
<th>Post-Port (V1.4.1) SLOC</th>
<th>Reused SLOC</th>
<th>Changed SLOC</th>
</tr>
</thead>
<tbody>
<tr>
<td>QPSK Assembly Controller</td>
<td>4087</td>
<td>2766</td>
<td>1173</td>
<td></td>
</tr>
<tr>
<td>QPSK IO</td>
<td>4307</td>
<td>2990</td>
<td>1332</td>
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<tr>
<td>QPSK MAC</td>
<td>4635</td>
<td>3333</td>
<td>1311</td>
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</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>13029</strong></td>
<td><strong>9089</strong></td>
<td><strong>3816</strong></td>
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<table>
<thead>
<tr>
<th>DSP Component</th>
<th>Pre-Port (V1.3) SLOC</th>
<th>Post-Porting (V1.4.1) SLOC</th>
<th>Reused SLOC</th>
<th>Changed SLOC</th>
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<tbody>
<tr>
<td>QPSK Physical</td>
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<td>2348</td>
<td>458</td>
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</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>100%</strong></td>
<td><strong>85%</strong></td>
<td><strong>17%</strong></td>
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</table>
QPSK Porting Issues

Porting of the QPSK WF encountered the following issues:

- The change from single process to multi-process memory model forced changes in implementation of Portable Object Adapter (POA) and use of Global variables
- Native vs. Environment Variable for exception handling
- Include path Issues related to development tools environment differences (i.e. case sensitivity)
- DSP Resource Sizing and Processor Utilization
  - Movement of filter for I&Q data to FPGA
**FM3TR Overview**

- The FM3TR waveform is an international test waveform initially developed by the Air Force Research Labs (AFRL).

- The FM3TR waveform provides:
  - Frequency hopping (250 hops per second / hop every 4 ms)
  - VHF and UHF military bands (30 MHz- 400 MHz)
  - Voice capability utilizing CVSD modulation for voice digitizing
  - Specification contains data capability

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![FM3TR Overview Diagram](image-url)
## FM3TR SLOC Metrics

<table>
<thead>
<tr>
<th>GPP Components</th>
<th>Pre-Port (V2.1) SLOC</th>
<th>Post-Port (V2.2.1) SLOC</th>
<th>Reused SLOC</th>
<th>Modified and New SLOC</th>
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<td>FM3TR Assembly Controller</td>
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<td>FM3TR MAC</td>
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<td><strong>Total</strong></td>
<td>6,304</td>
<td>6,285</td>
<td>1,403</td>
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<tr>
<td></td>
<td>100%</td>
<td>99%</td>
<td>22%</td>
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<thead>
<tr>
<th>DSP Component</th>
<th>Pre-Port (V2.1) SLOC</th>
<th>Post-Porting (V2.2.1) SLOC</th>
<th>Reused SLOC</th>
<th>Modified and New SLOC</th>
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<tr>
<td>FM3TR Physical</td>
<td>2,342</td>
<td>2,206</td>
<td>472</td>
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<tr>
<td></td>
<td>100%</td>
<td>94%</td>
<td>20%</td>
<td></td>
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Porting of the QPSK WF encountered the following issues:

- Changes to configuration of Portable Object Adapter caused by the difference of memory model
  - Flat memory model vs. Separate memory model.
- Changes caused by difference of byte order (endian)
- Changes of exception handling
  - Use of CORBA Environment Variable vs. native exception handling
- Changes of stub and skeleton file name related to difference of development tool
Summary

- USA-Japan Gov’t to Gov’t MOU to demonstrate SCA with international partner in 2002
- Program started in 2003 with SCA introduction to Japan
- SDR HW and OE development in 2004
- Successful SCA compliance testing of both Operational Environments (OE) - CF, RTOS, CORBA middleware
  - USA Radio OE (Raytheon CF) certified in Dec 05 - DoD Cluster 2 Handheld.
  - Japan Radio OE successfully tested for SCA 2.2 compliance in Jan 2005
  - Approximately 2 weeks each for certification period
- QPSK and FM3TR development in 2004-2005
Summary (cont.)

- Successful completion of QPSK & FM3TR ports in 2006
- Successful SCA compliance testing of both waveforms
  - Included performance and interoperability testing
  - QPSK Porting Metrics
    - 70% Code Reuse
    - 3 calendar months approx. 12 mm
  - FM3TR Porting Metrics
    - 90% Code Reuse
    - 3 calendar months approx. 9 mm
- Delivery of FM3TR & QPSK documentation (WDS, SDD, SRS, etc.)
- Performed Japan–USA Over-the-Air interoperability demos in Nov. 2006
Conclusion